LOW FREQUENCY NOISE SOURCES IN BIPOLAR JUNCTION TRANSISTORS

By
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By

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Major Department: Electrical Engineering

This dissertation is concerned with the sources of low frequency noise in bipolar junction transistors. Noise measurements on silicon planar diffused transistors indicate that the present noise model inadequately represents the noise performance of modern transistors.

An improved noise model is presented which includes three distinct excess noise sources. Two of the noise sources have a 1/f noise spectrum. One represents noise generated at the surface of the transistor; the other represents noise generated in the emitter-base space charge region. The importance of the third source of low frequency noise, burst noise, has only been recognized recently since the advent of monolithic integrated circuits. Burst noise consists of sudden discrete shifts in the dc collector current of the transistor. The erratic behavior of this noise can severely impair the performance of high gain integrated amplifiers. The electrical behavior of burst noise is experimentally investigated and a phenomenological noise generator is developed.

A transistor amplifier configuration utilizing two transistors and a dc current source is analyzed using this improved noise model. Both the analytical and experimental results show that this configuration is capable of dramatically reducing the effects of the low frequency noise sources of bipolar junction transistors.

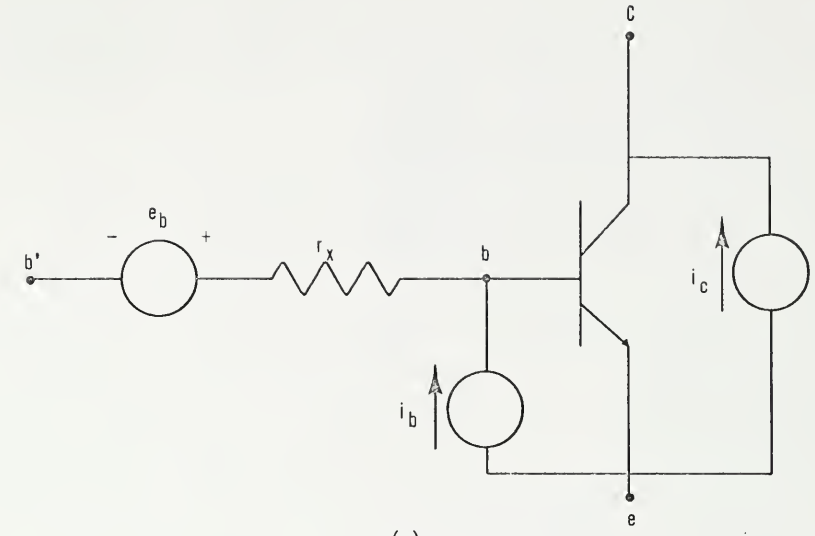
CHAPTER ONE

INTRODUCTION

Historical Background

Theory of the low frequency noise performance of the bipolar junction transistor has existed for many years and has remained essentially unchanged since its inception (1, 2, 3). The essence of the shot and thermal noise performance of the transistor is shown in Fig. 1-1a. The shot noise of the intrinsic transistor may be represented by a shot noise generator i_b in parallel with the base-emitter junction and a shot noise generator i_c in parallel with the collector-emitter terminals of the transistor. Also shown in Fig. 1-1a is the thermal noise generator e_b associated with the extrinsic base resistance of the device. The low frequency 1/f noise of the transistor may be represented by a flicker noise generator in parallel with the emitter-base junction of the transistor as developed by Fonger (4). The basic low frequency noise performance of the transistor is represented in the model of Fig. 1-1b.

The source of the 1/f noise represented by the above noise generator has been a source of considerable conjecture. Fonger originally associated 1/f noise with fluctuations in current recombining at the base surfaces. More recently Sah (5) and others (6) have shown



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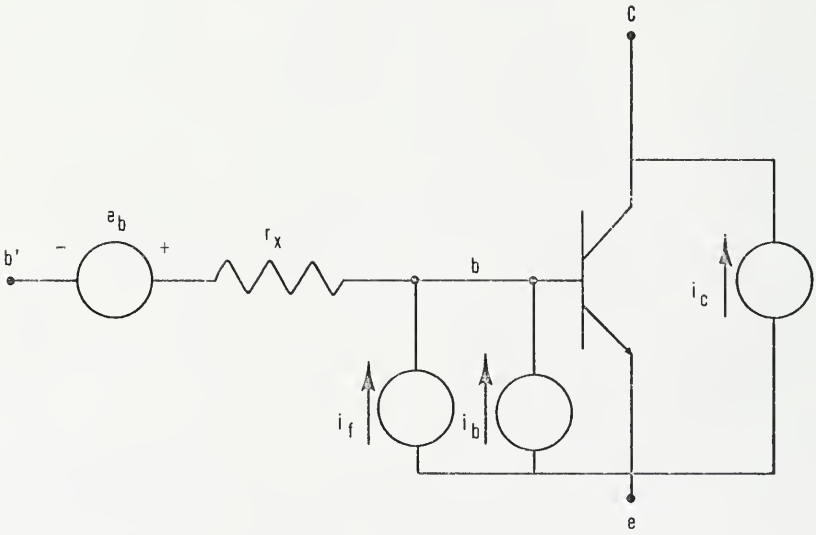

(b)

Fig. 1-1. Basic transistor noise model.

more experimental evidence supporting the surface noise theory. Gibbons (7) has suggested that the source of 1/f noise in low noise transistors is the emitter-base transition region rather than the surfaces of the device. Knott (8) recently concluded that there is 1/f noise originating within the transistor. Investigation is clearly needed to determine whether more than one 1/f noise generator exists in the transistor and to determine the proper location in a transistor noise model of the generators which are found to exist.

Another noise phenomenon, burst noise, has been entirely neglected in the transistor noise model. Originally noticed in carbon resistors and reverse-biased p-n junctions, burst noise has only recently been recognized as a problem in transistors (9, 10). With the advent of integrated circuits, and their associated yield problems, the luxury of ignoring or disposing of bursting units can no longer be afforded. One can no longer select special low noise units with which low noise amplifiers may be constructed, but must accept the performance of the transistors comprising the integrated amplifier. Thus burst noise cannot be tolerated in low noise integrated amplifiers. The breadth of this problem and lack of available information about burst noise indicate that a study of this phenomenon is needed. This noise form is neglected in the noise model of Fig. 1-1, and a generator characterizing the effects of burst noise should be included in any complete low frequency noise model of the transistor.

Both burst noise and 1/f noise reduce the sensitivity of amplifiers at low frequencies. The present method of controlling 1/f noise is to attempt to produce transistors having "clean" surfaces and oxides

by careful process control. At this time there is no known method of controlling burst noise. Investigation is needed to determine if circuit techniques exist through which the 1/f and burst noises may be controlled.

Low Frequency Noise Model of the Transistor

The Hybrid-Pi small signal model of the transistor was chosen as the transistor model to be used in this study (11). The above model was chosen because it provides both an accurate description of the performance of the transistor over a wide frequency range and insight into the physical processes which occur in the transistor. The Hybrid-Pi model of the transistor is shown in Fig. 1-2. A noise model of the transistor is easily generated by superimposing the four noise generators discussed earlier on the model of Fig. 1-2. The resulting noise model of the transistor is shown in Fig. 1-3.[1] The two current generators i_b and i_c are noise generators showing the full shot noise of the base and collector currents respectively. The generator i_f is a phenomenological noise generator which describes the noise performance of the transistor in the 1/f noise region. The noise emf e_b is a generator which represents the full thermal noise of the base resistance r_x. The above generators can be described by the formulation below (12).

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[1] The model of Fig. 1-3 tacitly assumes that the transistor bias currents are much greater than its leakage currents and that the transistor has reasonably high beta.

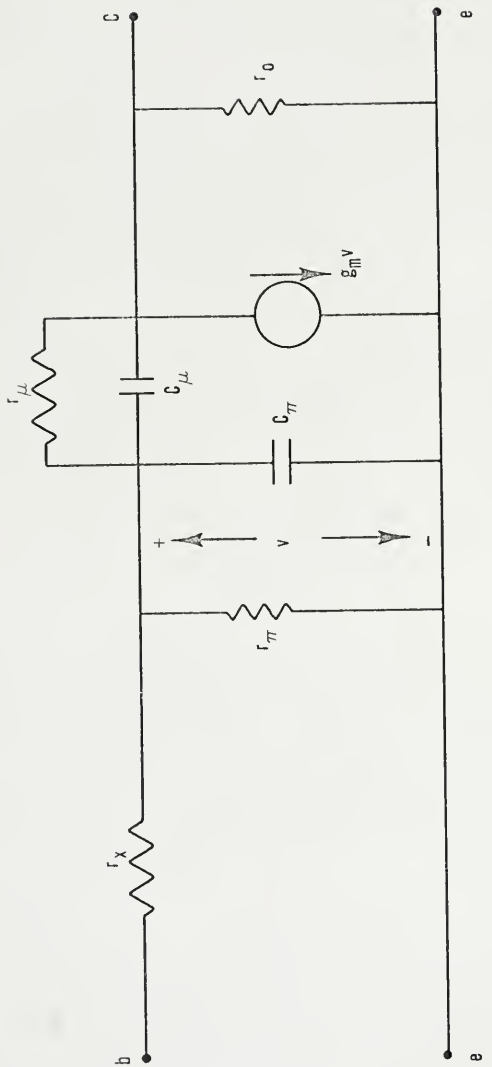


Fig. 1-2. Hybrid-Pi small signal model of the transistor.

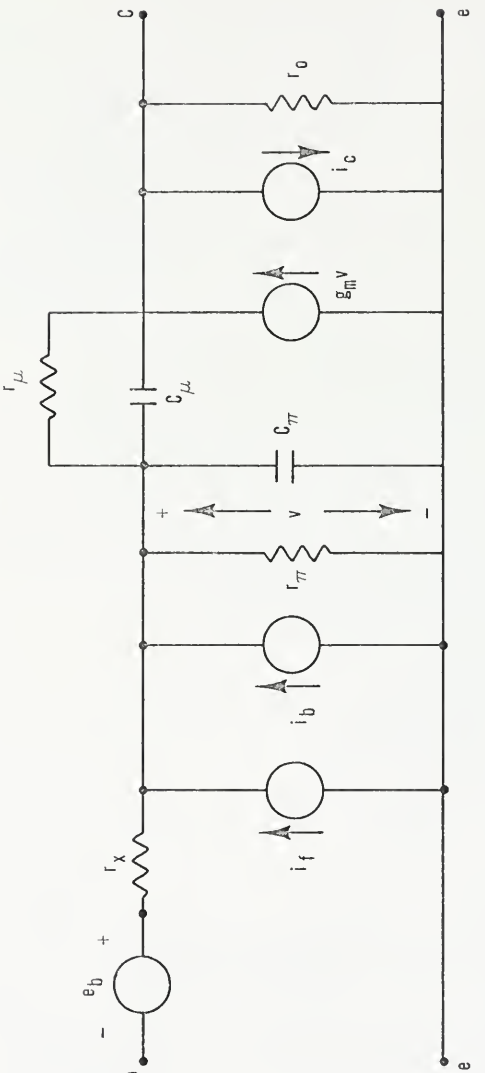


Fig. 1-3. Noise model employing the Hybrid-Pi model of the transistor.

$$\overline{i_b^2} = 2qI_C df \quad (1.1)$$

$$\overline{i_c^2} = 2qI_B df \quad (1.2)$$

$$\overline{e_b^2} = 4kTr_x df \quad (1.3)$$

$$\overline{i_f^2} = KI_B df/f \quad (1.4)$$

For low frequencies the model of Fig. 1-3 may be considerably simplified. At low frequencies the effects of C_π and C_u are unimportant, and these capacitors may be deleted from the model. The resistor r_u affects the gain of the transistor only when the device is operated under conditions of high voltage gain and may also be neglected. The result of these simplifications is the model of Fig. 1-4. The model of Fig. 1-4 will be the low frequency noise model used throughout this noise study.

Summary

The purpose of this work as developed above is twofold. First the 1/f and burst noise phenomenon are to be studied and modeled, and then methods of controlling these two noise forms are to be investigated.

Chapter Two presents the results of an experimental study of 1/f noise beginning with the above low frequency noise model and resulting in the development of an improved noise model which more fully explains the noise performance of the transistor in the 1/f noise region.

Chapter Three presents the results of a study of burst noise including modeling of burst noise by a burst current generator, determination of the functional dependence of this generator, and qualitative ideas as to the origin of the burst noise phenomenon.

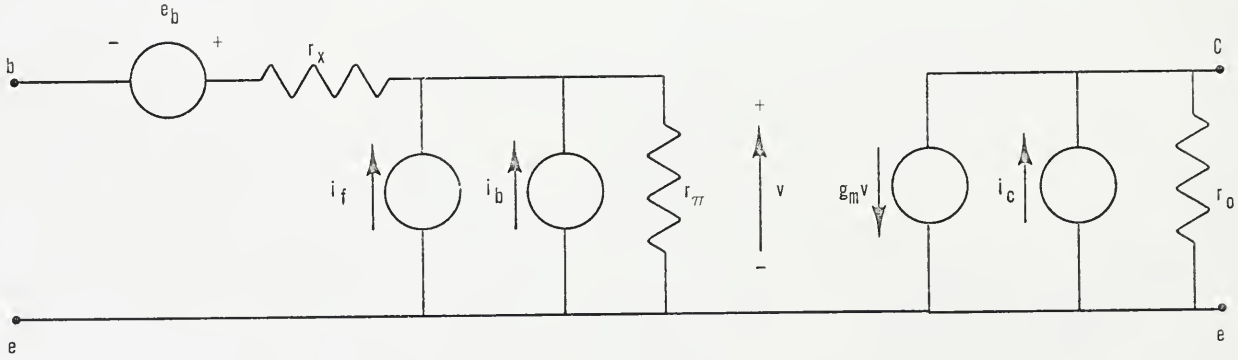


Fig. 1-4. Simplified low frequency noise model of the transistor.

A low noise amplifier configuration is presented in Chapter Four. This amplifier should provide a method of realizing low frequency low noise amplifiers whose noise resistance is basically limited by the thermal noise of the base resistances of the transistors comprising the amplifier and by the shot noise of the collector current of the second transistor of the amplifier configuration. This amplifier also provides a method of effective control of burst noise.

Results of this study and recommendations for further work indicated by this study are presented in Chapter Five.

CHAPTER TWO

1/f NOISE SOURCES IN BIPOLAR JUNCTION TRANSISTORS

Noise Figure and Equivalent Noise Resistance

In any noise study it is necessary to have a noise measure which may be used to compare the noise performance of various noisy devices. Two common and convenient measures are equivalent noise resistance R_n and noise figure F. Equivalent noise resistance and noise figure, developed below, will be used to characterize the noise performance of devices throughout this thesis.

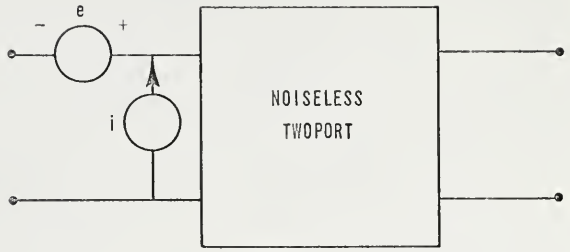
The noise of a twoport may be conveniently represented by two noise sources as shown in Fig. 2-1a (13, 14). For a given input termination R_s, the equivalent circuit of the twoport may be further reduced to the circuit of Fig. 2-1b in which the noise source e_t is given by

$$e_t = e + iR_s \quad . \tag{2.1}$$

The total mean square noise voltage $\overline{e_n^2}$ at the input of the twoport may be computed with the aid of Nyquist's theorem (15),

$$\overline{e_n^2} = \overline{e_t^2} + 4kTR_s df \tag{2.2}$$

and can be represented by the equivalent circuit of Fig. 2-1c in which R_s is now a noiseless resistor. The noise emf e_n may be expressed as an equivalent noise resistance defined by



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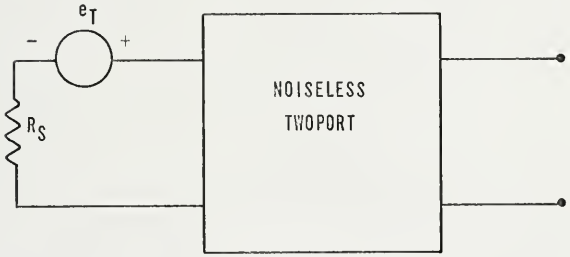

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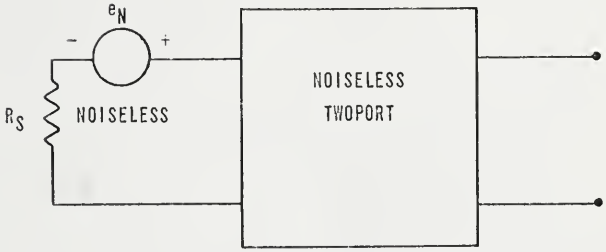


(c)

Fig. 2-1. Representation of a noisy twoport.

$$R_n = \overline{e_n^2}/4kTdf \quad . \tag{2.3}$$

In this form, the equivalent noise resistance R_n is a convenient quantity by which various noisy devices may be compared. Noise figure F may be defined in terms of the equivalent noise resistance R_n and is given by the formula below (16).

$$F = R_n/R_s \tag{2.4}$$

Thus equivalent noise resistance R_n provides both an effective method of comparing the noise performance of various devices and a method of determining the corresponding noise figure F.

Measurement of equivalent noise resistance R_n can be accomplished using a sinusoidal comparison technique (17). Figure 2-2 shows the basic measuring system consisting of the device under test, a sinusoidal calibrating signal, a noiseless variable gain amplifier, a filter, and a quadratic detector.

The device under test may be represented by an equivalent noise resistance followed by a noiseless twoport having a gain A as shown in Fig. 2-3. The equivalent noise resistance R_n may be determined using the following procedure. With the switch in position one, the reading M1 of the detector will be

$$M1 = (4kTR_n df)^{1/2} A1 \cdot AV1 \quad . \tag{2.5}$$

With the switch in position two and with the amplifier gain set to the second gain setting, the detector reading M2 is obtained.

$$M2 = (\overline{e_{cal}^2} + 4kTR_n df)^{1/2} \cdot A1 \cdot AV2 \tag{2.6}$$

Choosing the calibrating signal such that $M_2 = M_1$:

$$(\overline{e_{cal}^2} + 4kTR_n df)A1^2AV2^2/(4kTR_n df)A1^2AV1^2 = 1. \tag{2.7}$$

This may be easily solved for noise resistance R_n yielding

$$R_n = \overline{e_{cal}^2}/(4kTdf)\ (AV1/AV2)^2(1-(AV2/AV1)^2) \quad . \tag{2.8}$$

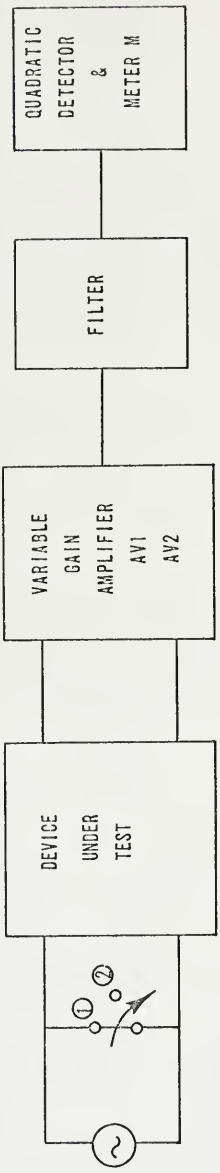


Fig. 2-2. Basic noise measurement system.

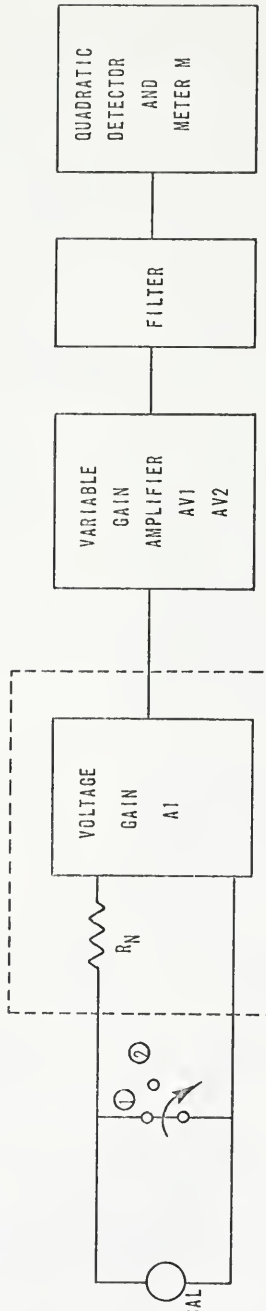


Fig. 2-3. System for measuring equivalent noise resistance.

The value of noise resistance R_n is determined using the above equation.

Low Frequency Noise Performance of the Transistor as Predicted by the Existing Noise Model

The low frequency noise model of Chapter One is shown in Fig. 2-4. The noise figure of the transistor obtained from this model is

$$F = 1 + r_x/R_s + g_m(R_s+r_x)^2/2h_{FE}R_s + g_m(R_s+r_x+\beta_o/g_m)^2/2R_s\beta_o^2 + \overline{i_f^2}(R_s+r_x)^2/4kTR_s df \quad . \tag{2.9}$$

The above expression may be simplified by considering two noise regions; a region in which the 1/f noise generator dominates the transistor noise performance, and a region in which shot and thermal noise generators are dominant. The resulting expression for noise figure in the shot noise region is

$$F = 1 + r_x/R_s + g_m(R_s+r_x)^2/2h_{FE}R_s + g_m(R_s+r_x+\beta_o/g_m)^2/2R_s\beta_o^2. \tag{2.10}$$

This expression for the noise figure in the shot noise region has a minimum value F_{min} given below (18).

$$F_{min} = 1 + g_m(r_x+Rs_{min})/h_{FE} \tag{2.11}$$

$$Rs_{min} = [(h_{FE}(1 + 2g_m r_x + (g_m r_x)^2/h_{FE}))]^{1/2}/g_m \tag{2.12}$$

The noise figure of the transistor may be minimized by the proper selection of source resistance R_s. For a given value of r_x, the noise figure may be computed in the shot noise region, and the model of Fig. 2-4 may be verified for the shot noise region.

In the 1/f noise region the 1/f noise generator dominates the noise performance, and the noise figure expression of Eqn. 2.9 reduces to the expression

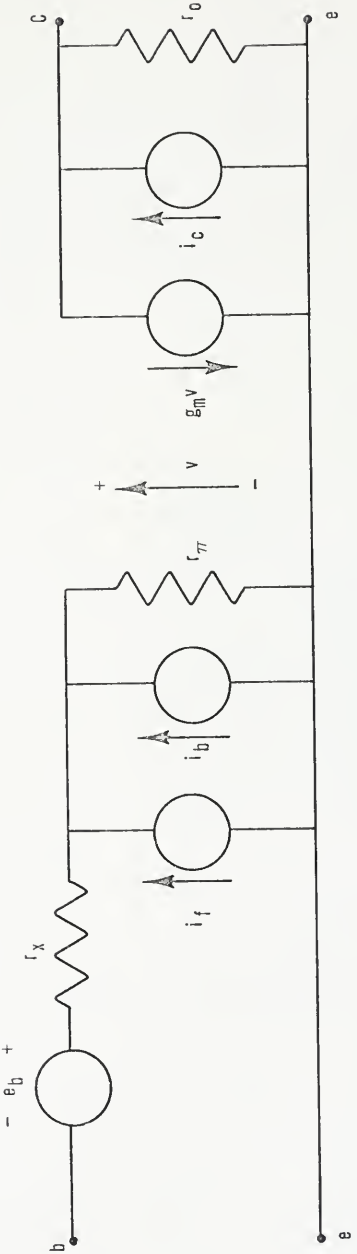


Fig. 2-4. Simplified low frequency noise model of the transistor.

$$F = 1 + \overline{i_f^2}(R_x+r_x)^2/4kTR_s df \quad . \tag{2.13}$$

This expression may also be minimized by proper choice of source resistance R_s.

$$F_{min} = 1 + \overline{i_f^2}(r_x/kTdf) \qquad \text{for} \tag{2.14}$$

$$R_{smin} = r_x \tag{2.15}$$

Noise figure measurements in the 1/f noise region may thus be used to determine the value of the base resistance r_x of the model of Fig. 2-4.

The noise figure in the 1/f noise region must be of a sufficient magnitude to insure accuracy of the measurements of r_x using the above method. The sufficient magnitude is determined below. For the model of Fig. 2-5, the noise figure is easily determined to be

$$F = 1 + r_x/R_s + M(R_s+r_x)^2/R_s \quad , \quad M = \overline{i_f^2}/4kTdf + \frac{g_m}{2h_{FE}} \tag{2.16}$$

which has a minimum for

$$R_{smin} = (r_x^2 + r_x/M)^{1/2} \quad . \tag{2.17}$$

Manipulation yields

$$r_x^2 = R_s^2/\left[1 + 4F_{min}/(F_{min}-1)^2\right] \quad . \tag{2.18}$$

Thus for r_x to be determined within one percent, F_{min} in the 1/f noise region must be at least 202. A minimum noise figure of 20 is required if r_x is to be determined within ten percent.

Measurements of noise figure versus source resistance in the 1/f noise region can be used to help characterize the model of Fig. 2-4. The base resistance r_x may be easily determined by noise measurement in the 1/f noise region. Then, knowing r_x, the minimum noise figure and source resistance corresponding to this minimum may be calculated for the shot noise region. Measurements in the shot noise region may then be used to check the validity of the noise model of Fig. 2-4.

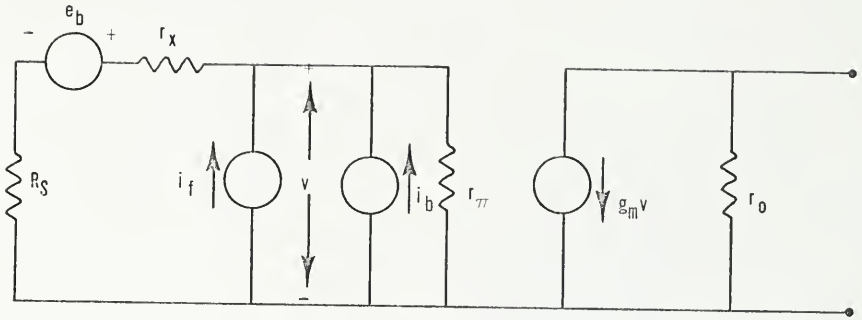


Fig. 2-5. Noise model for determination of accuracy of base resistance measurements.

The apparent validity of the preceding noise theory is demonstrated by unit CA-3018-876. Measurements of noise figure versus source resistance in the 1/f noise region yield a value of r_x = 560 ohms as indicated in Fig. 2-6. Measurements of F versus R_s in the shot noise region yield values of F_{min} and R_{smin} of 1.26 and 5 kohms respectively, also shown in Fig. 2-6. Values of R_{smin} and F_{min}, 5.6 kohms and 1.24 respectively, predicted using Eqns. 2.11 and 2.12 with the above values of r_x, show excellent agreement with the above measurements. Small signal measurements yield a value of r_x = 545 ohms. Thus the noise model of Fig. 2-4 correctly predicts the low frequency noise performance of the transistor tested, and the 1/f noise generator sees the same base resistance as the base current shot noise generator.

Breakdown of the Existing Noise Model

The transistor discussed above demonstrated very good agreement with the accepted noise model and its theory. However, low frequency noise measurements upon other transistors have shown little agreement with the above theory. The 1/f noise generator above sees the total base resistance r_x, and the minimum noise figure in the 1/f noise region should occur for a source resistance R_s equal to the base resistance r_x. In most cases, as shown by the typical unit of Fig. 2-7, the value of r_x obtained by small signal measurements disagrees greatly with that obtained from noise measurements in the 1/f noise region. Unit Z has a base resistance value of 7.8 kohms determined by small signal measurements, but the indicated value of r_x determined from Fig. 2-7 is 2.7 kohms.

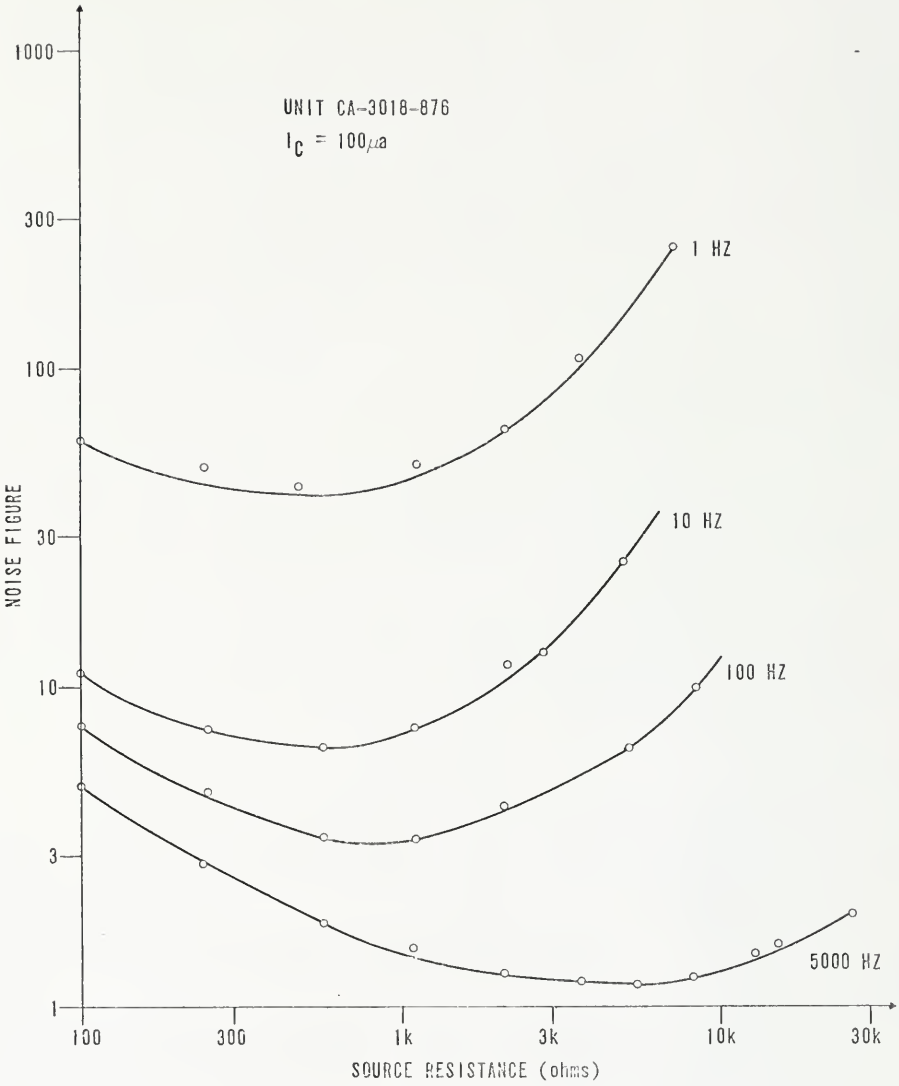


Fig. 2-6. Noise figure versus source resistance for CA-3018-876.

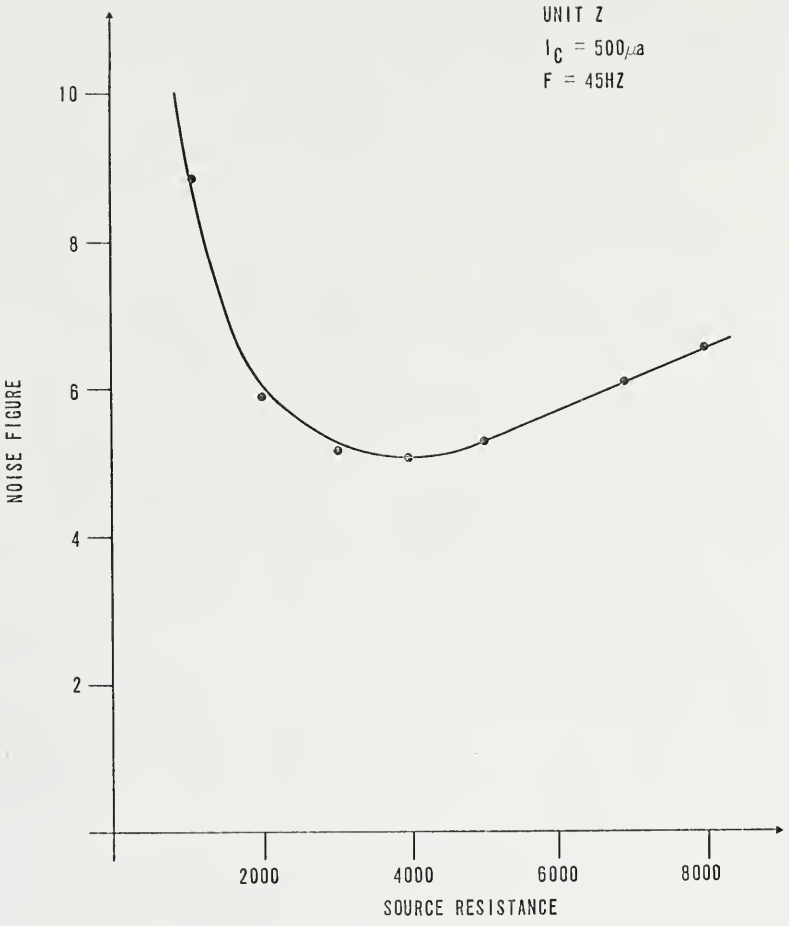


Fig. 2-7. Noise figure versus source resistance for unit Z.

The origin of this discrepancy was studied further by producing special four terminal devices, tetrode transistors, in the Microelectronics Laboratory of the University of Florida. The geometry of the tetrodes is shown in Fig. 2-8. The fourth electrode consists of a field plate or gate physically located over the emitter-base junction of the transistor. By applying a potential to the gate the carrier densities at the surface of the transistor under the gate can be altered, and any mobile ions in the oxide under the gate may be affected. It is also known that a potential on this gate will affect the 1/f surface noise of the device (19, 20).

Measurements of noise figure versus frequency for device #195 are shown in Fig. 2-9. As the gate voltage is increased, the 1/f noise of the device increases greatly as expected. Measurements of noise figure versus source resistance for device #195 are shown in Fig. 2-10. The value of R_{smin} of these figures varies widely as the gate potential and hence 1/f surface noise varies. The variations above may be accounted for through the model develcped below.

An Improved Noise Model Including Two 1/f Noise Generators

Consider the noise model of Fig. 2-11 in which two 1/f noise generators are shown. The noise figure in the 1/f noise region is found to be

$$F = 1 + \overline{i_{f1}^2}(R_s+r_a)^2/4kTR_s df + \overline{i_{f2}^2}(R_s+r_x)^2/4kTR_s df . \quad (2.19)$$

Again the expression for noise figure may be minimized through the proper choice of R_s.

$$R_{smin} = [(r_a^2 + \varepsilon r_x^2)/(1+\varepsilon)]^{1/2} , \quad \varepsilon = \overline{i_{f2}^2}/\overline{i_{f1}^2} . \quad (2.20)$$

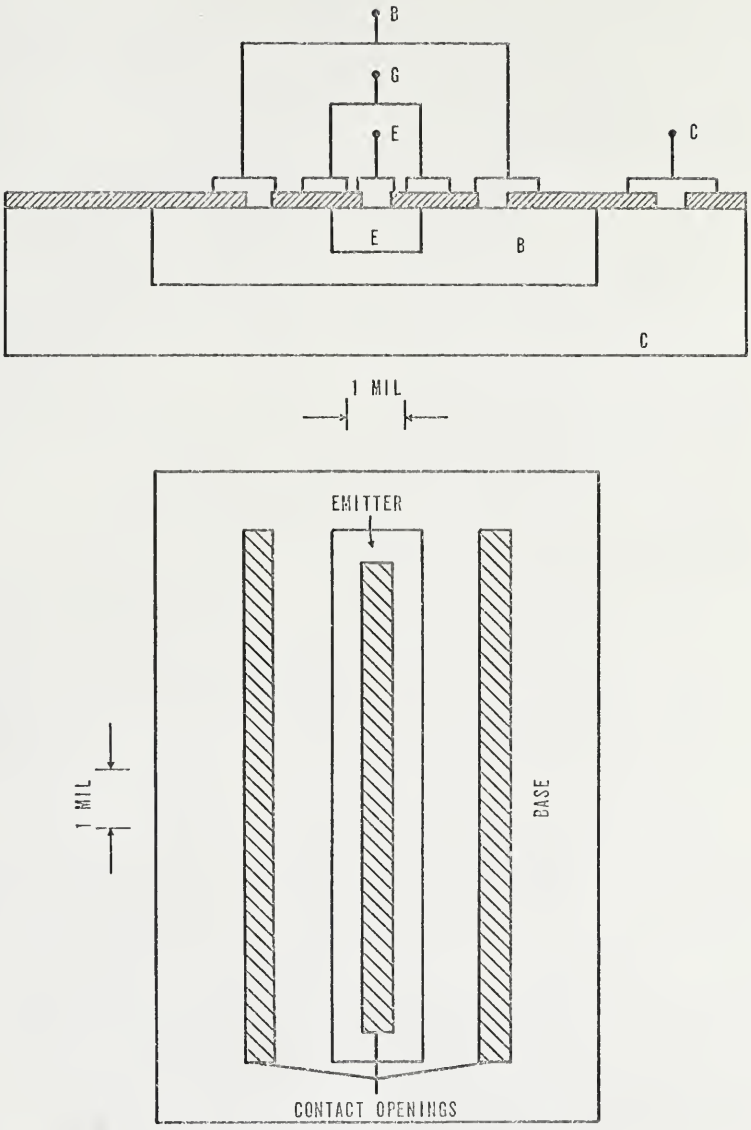


Fig. 2-8. Tetrode transistor structure.

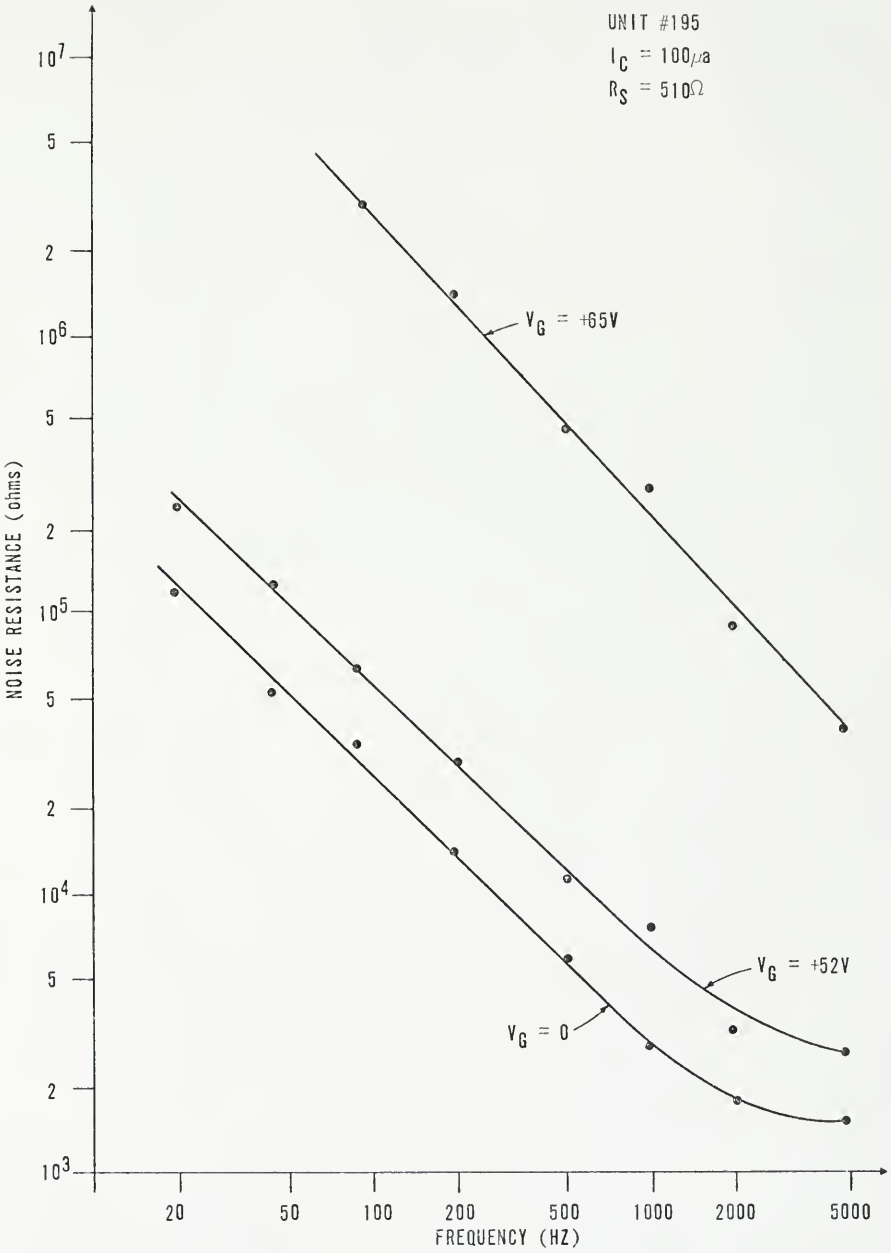


Fig. 2-9. Noise resistance versus frequency with gate voltage as a parameter for device # 195.

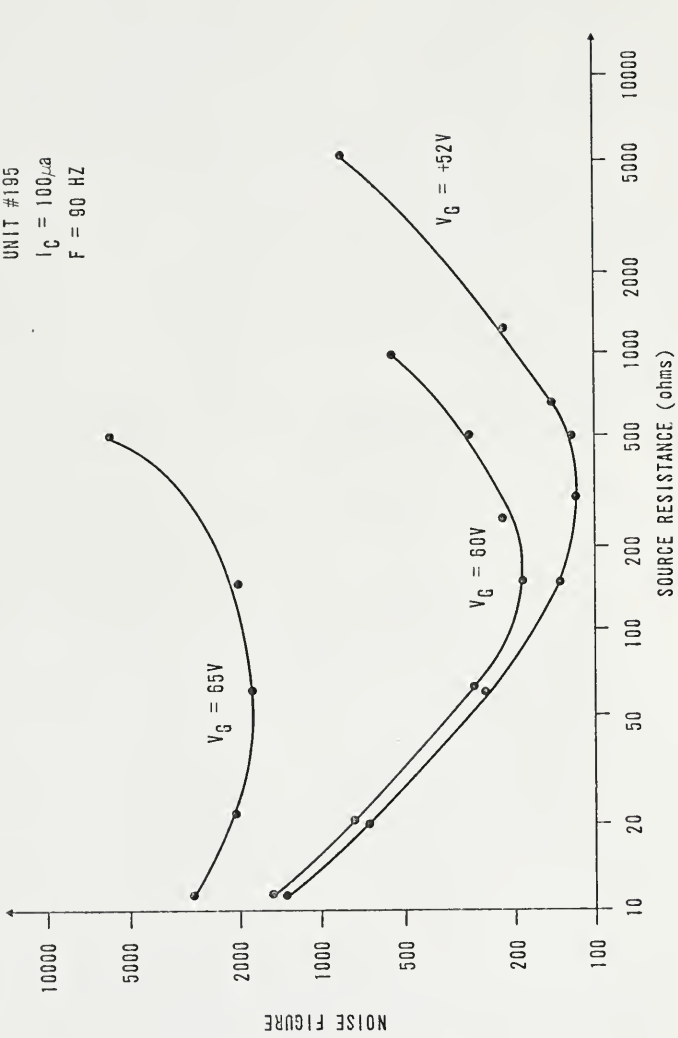


Fig. 2-10. Noise figure versus source resistance with gate voltage as a parameter for device # 195.

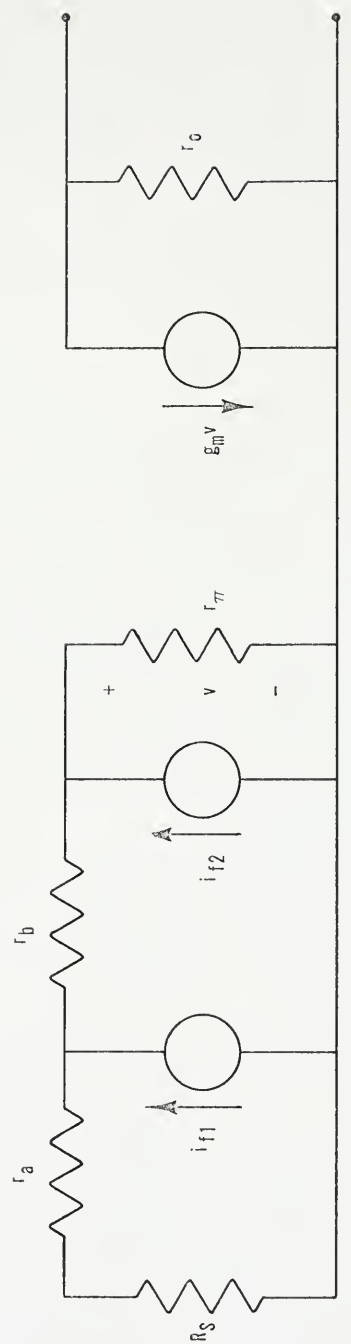


Figure 2-11. Improved low frequency noise model for the 1/f noise region.

Two cases of Eqn. 2.19 emerge, depending upon the dominance of either i_{f1} or i_{f2} as shown below.

For i_{f1} sufficiently large,

$$R_{smin} = r_a \quad \text{and} \quad F_{min} = 1 + \overline{i_{f1}^2} r_a / kTdf \quad . \tag{2.21}$$

For i_{f2} sufficiently large,

$$R_{smin} = r_x \quad \text{and} \quad F_{min} = 1 + \overline{i_{f2}^2} r_x / kTdf \quad . \tag{2.22}$$

As the ratio of the two noise sources, ε, varies, R_{smin} varies between the values r_a and r_x. The values of r_x and r_a may be determined as discussed below.

Earlier measurements have confirmed the validity of the model of Fig. 2-4 for some transistors. In that model it was seen that the 1/f noise generator and the shot noise generator shared the same position in the model. This generator should then be associated with the active base region of the device. As discussed in Chapter One, the existence of a generator in this location has been alluded to in the past. Other measurements have associated 1/f noise with the transistor surfaces, particularly near the surface of the emitter-base junction. The approximate position of the above generators can be determined from the device geometry as shown in Fig. 2-12. The total base resistance r_x of a transistor may be divided into two parts: a portion due to the inactive base region between the base contacts and the edges of the emitter and a portion corresponding to the active base region under the emitter of the transistor as shown in Fig. 2-12 (21). A noise generator associated with the surface of the emitter-base junction should see only a portion of the base resistance corresponding to the inactive base region rather than the total base resistance of the device. On the other

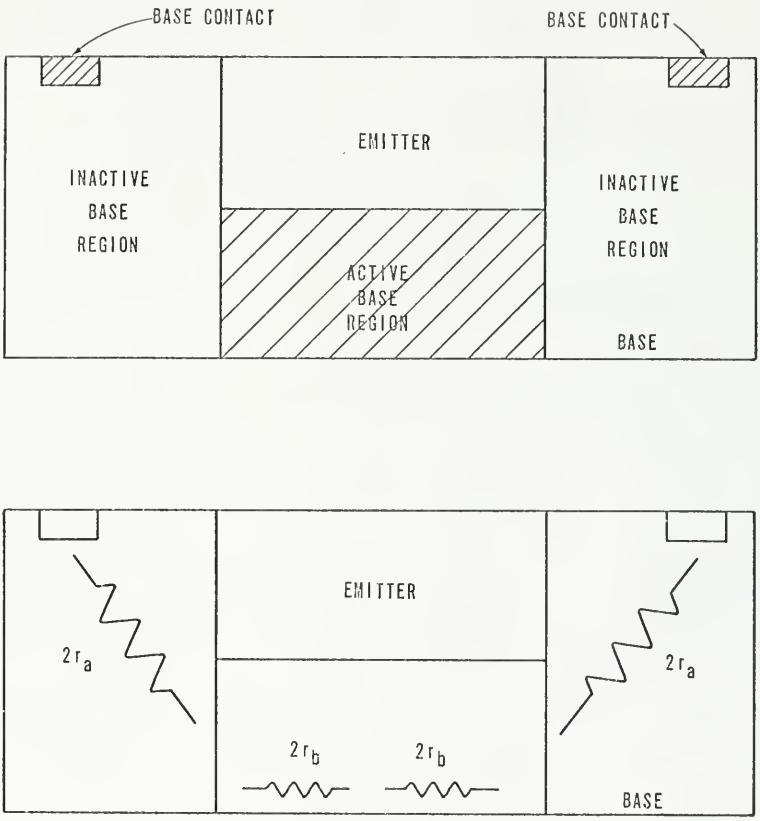


Fig. 2-12. Transistor structure showing two components of the base resistance of a transistor.

hand a noise generator associated with the active base region would see the total base resistance of the device.

The base resistances of Fig. 2-11 can now be determined. The resistance r_a is approximately the base resistance due to the inactive base region, and the sum $r_a + r_b$ is equivalent to the total base resistance of the device so that

$$r_x = r_a + r_b \,. \tag{2.23}$$

Measurements upon device #195 determine the values of r_a and r_b of the model of Fig. 2-11. The geometry of the tetrode transistor indicates that there is 1/18 square of material in the inactive base region. Sheet resistivity measurements for device #195 yield a value of 180 ohms per square for this region and hence a value of 10 ohms for the value of r_a. Small signal input impedance measurements indicate a value of 650 ohms for the total base resistance r_x yielding a value of 630 ohms for r_b. The measurements given in Fig. 2-10 clearly show values of R_{smin} which fall within the range of 20-650 ohms. This performance is predicted by the model of Fig. 2-11 and the ratio ε of Eqn. 2.20 is effectively varied by varying the value of the gate potential on the tetrode.

Separate Dominance of the Two 1/f Noise Generators

The noise figure in the 1/f noise region for the improved noise model of Fig. 2-11 was given in Eqn. 2.19. If the noise generator i_{F2} is sufficiently dominant, the noise figure would be given by Eqn. 2.22. This was the case of the CA-3018 of Fig. 2-6. The case of dominance of the generator i_{f1} was developed in Eqn. 2.21, and is demonstrated below.

Device #147 was a specially treated device in which 1/f surface noise could be made the dominant noise form. Before metalization the oxide over the surface of the above transistor was contaminated with sodium ions by heating the transistor in a saturated salt solution at 95°C for twenty minutes. This treatment introduces mobile sodium ions into the oxide which may be later influenced by the potential on the gate electrode (22, 23). The completed transistor was subjected to heat treatment at a temperature of 200°C for fifteen minutes with the gate biased at first to plus fifty volts and then later at minus fifty volts with respect to the other electrodes. The heat treatment with the gate positive causes the mobile ions to drift toward the silicon-silicon dioxide interface, and with the gate negative the ions drift toward the gate electrode. The results of noise measurements upon the transistor with the ions drifted both toward and away from the transistor surface are shown in Fig. 2-13. With the ions drifted toward the gate electrode a structured spectrum was obtained. This will be discussed later. With the ions drifted toward the surface of the transistor, 1/f noise enhanced the noise spectrum by almost 20 db. Since the 1/f noise here was greatly influenced by the ions in the oxide under the gate the dominant source of this 1/f noise is the surfaces near the base-emitter junction of the transistor. Measurements of noise figure versus source resistance with the ions drifted toward the transistor surface are given in Fig. 2-14, and the indicated value of r_a of the model of Fig. 2-9 is 22 ohms. Sheet resistivity measurements yield a value of 10 ohms for the bulk material of the inactive base region for this device.

The above measurements show the existence of the two 1/f noise generators of Fig. 2-10 in which r_a is the resistance of the inactive

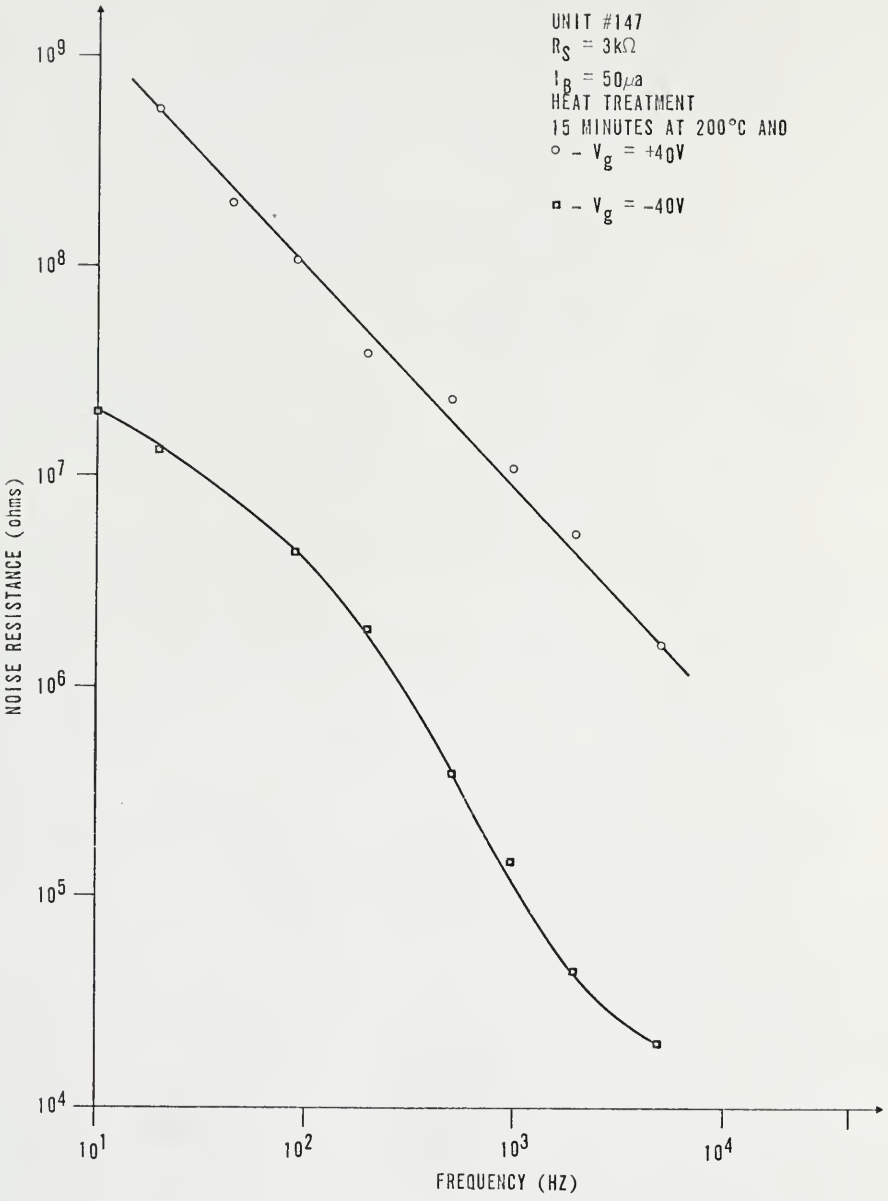


Fig. 2-13. Noise resistance versus frequency for device # 147.

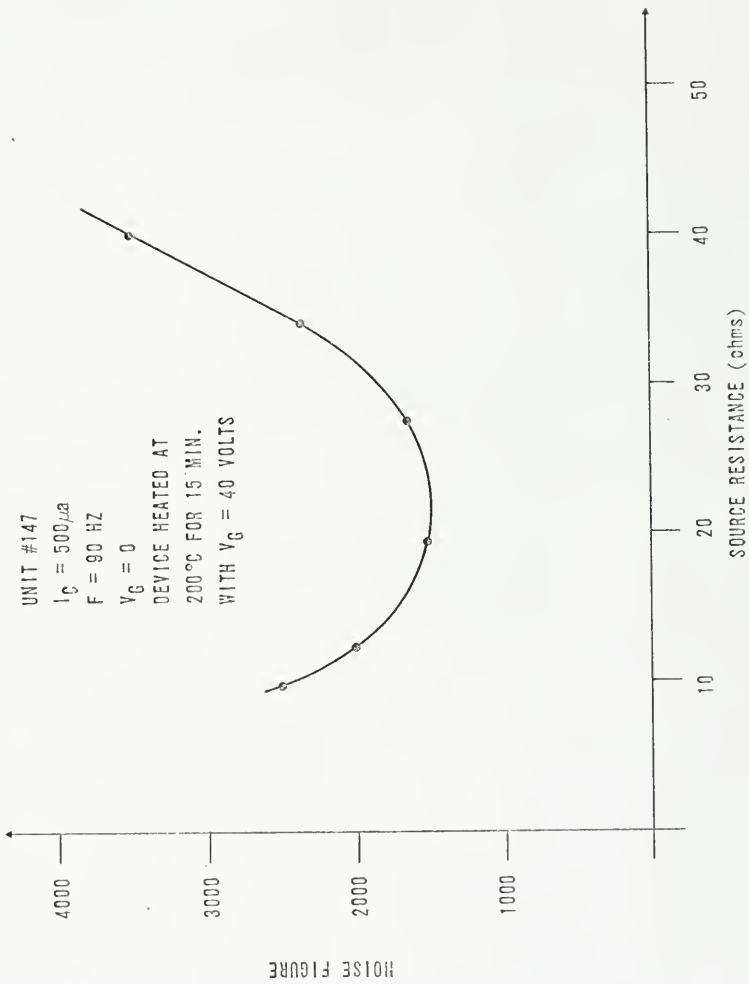


Fig. 2-14. Noise figure versus source resistance for device # 147.

base region, and the total base resistance of the transistor is given by

$$r_x = r_a + r_b \,. \tag{2.24}$$

CHAPTER THREE

BURST NOISE

Introduction

Typical burst noise waveforms are shown in Fig. 3-1. The waveforms shown are of collector current versus time and consist of sudden discrete shifts in the dc collector current of the transistor. The above phenomenon has long been observed in resistors and reverse-biased p-n junctions, and recently burst noise has been observed in the transistor.

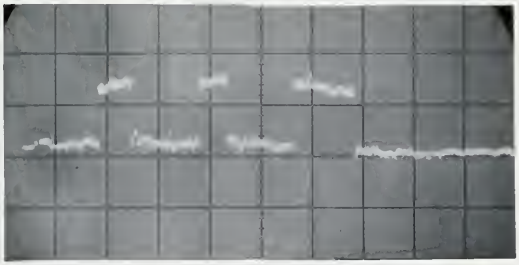
Burst noise has become a major problem in transistors only recently. In the past, one could select acceptable quiet devices with which low noise amplifiers could be constructed. In today's integrated circuit technology this procedure is no longer economically feasible, and burst noise has become a problem causing reduction of the yield of acceptable functioning integrated circuits.

The results of a study of the burst noise phenomenon are presented below.

Burst Noise Model and Spectral Representation

Burst noise has been shown to be a function of temperature, collector current, and source resistance, and to be independent of collector-base voltage (24, 25). The bursts are associated with the base-emitter

(a) 50 msec/cm



(b) 5 msec/cm

(c) 5 msec/cm

Fig. 3-1. Burst noise waveforms.

junction of the transistor, and the burst magnitude as measured at the collector of the transistor increases with increasing source resistance. The above knowledge leads to the modeling of burst noise by a burst current generator as shown in Fig. 3-2a. The functional dependence of this burst current generator will be discussed later. The current generator generates current pulses in the form of a random telegraph wave, and it sees some portion r_c of the total base resistance r_x. The functional dependence of the burst generator, i_{BB}, the value of the resistance r_c and hence the location of the burst generator, and the statistical representation of burst noise by a random telegraph wave are studied and determined below.

For a given operating point, the value of r_c may easily be determined. Taking a Thevenin equivalent of the generator i_{BB} and resistors R_s and r_c of Fig. 3-2a, the equivalent circuit of Fig. 3-2b is obtained in which an equivalent burst voltage generator e_{BB}, referred to the input of the transistor, is defined.

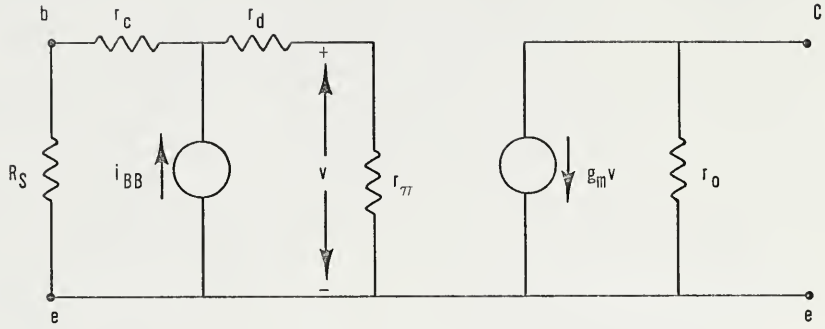
$$e_{BB} = i_{BB}(R_s+r_c) \tag{3.1}$$

Extrapolation of measurements of e_{BB} versus R_s will intersect the R_s axis at

$$R_s = -r_c \quad . \tag{3.2}$$

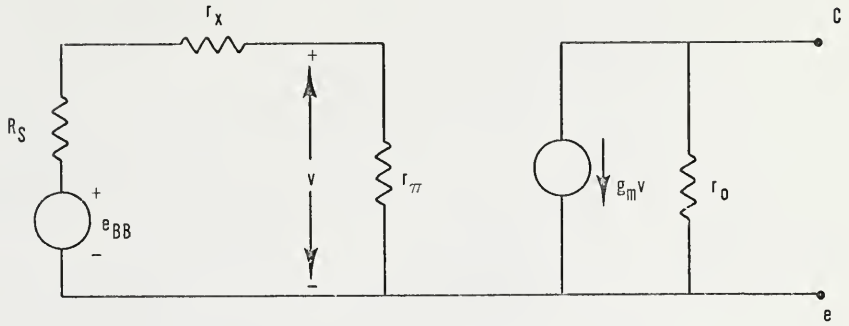
The position of the burst current generator can thereby be determined, as demonstrated below for unit #147.

Unit #147 was the treated unit discussed earlier. With the ions in the oxide drifted toward the gate electrode burst noise was very evident. Measurements of equivalent burst voltage yield a value of eight ohms for the resistor r_c of the noise model of Fig. 3-2b as



$$r_c + r_d = r_x$$

(a)



$$e_{BB} = i_{BB} (R_S + r_c)$$

(b)

Fig. 3-2. Burst noise model.

demonstratd in Fig. 3-3. As discussed earlier, the 1/f surface noise generator of this transistor saw a base resistance of approximately 22 ohms. Thus, within experimental error, both the burst noise and surface 1/f noise generators are located in approximately the same region near the surface of the emitter-base junction, and these two noise generators see approximately the same portion of the total base resistance of the device.

As mentioned earlier, burst noise may be modeled by a random telegraph wave as discussed below. Since the measuring apparatus removes the average value of the noise, the burst noise may be conveniently modeled by a random telegraph wave whose normalized power spectrum is given by

$$S(w) = 1/(1 + (\pi f/2a)^2) \quad , \tag{3.3}$$

in which a is the average number of bursts per second (26). The above power spectrum is shown in Fig. 3-4, and it has a value of one-half for $w = 2a/\pi$. The power spectrum of burst noise may be measured, and the results correlated with measurements of the average burst rate in order to confirm the supposition that burst noise can be represented by a random telegraph wave.

Verification of the random telegraph character of burst noise is demonstrated by device CA-3018-R-543. The low frequency noise of this device was dominated by burst noise, and the average burst rate was determined to be 369 bursts per second. The normalized noise spectrum of the burst noise should have a value of one-half for a frequency of 238 Hz. The measured power spectrum of the burst noise is presented in Fig. 3-5 and has the predicted shape and a half power frequency of

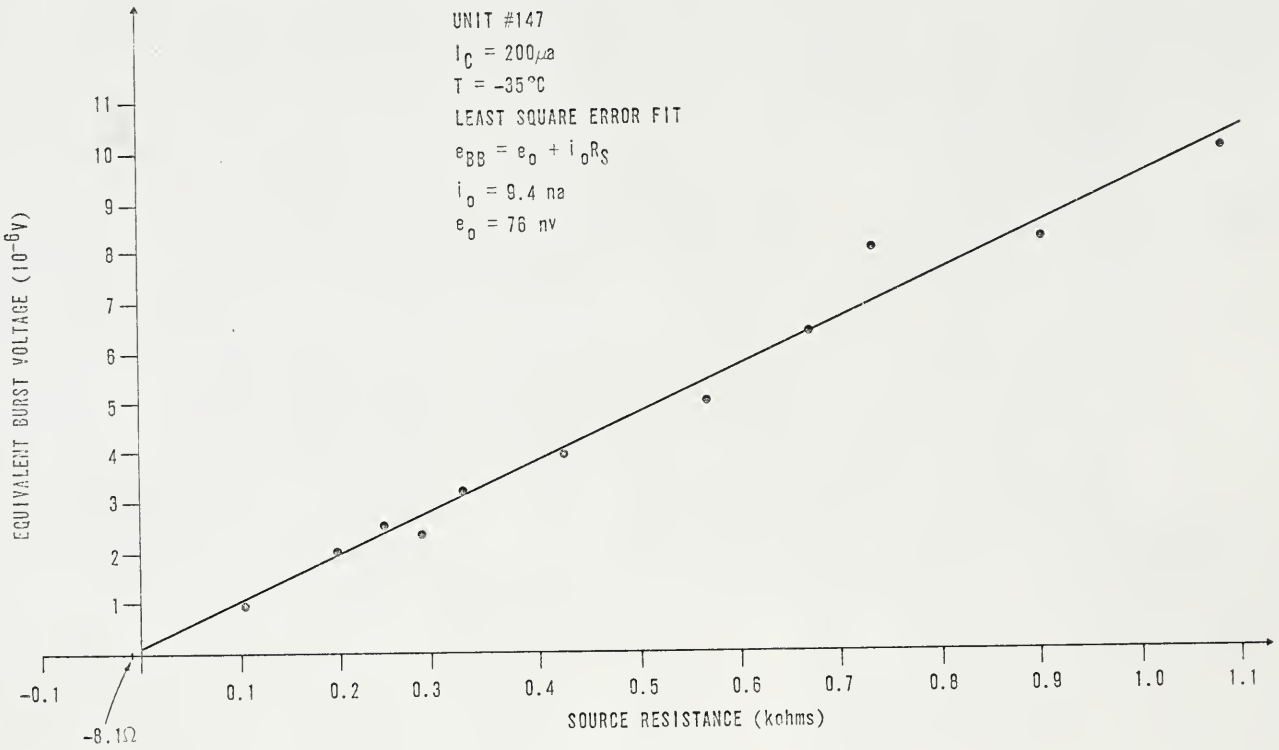


Fig. 3-3. Equivalent burst voltage versus source resistance.

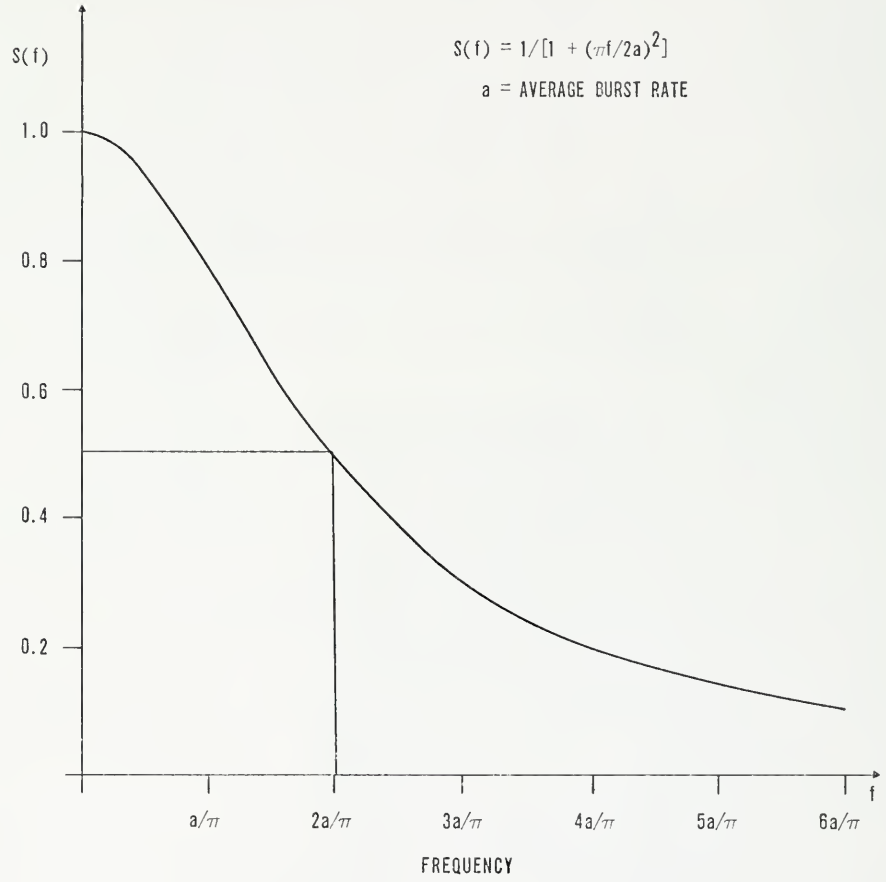


Fig. 3-4. Random telegraph wave spectrum.

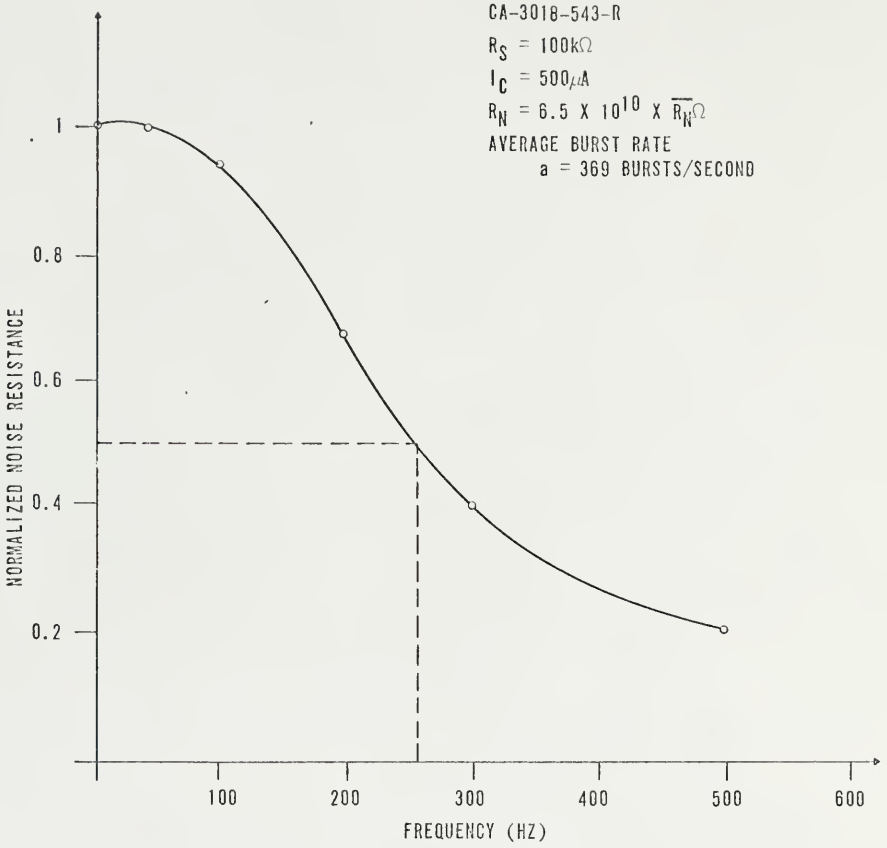


Fig. 3-5. Burst noise spectrum.

255 Hz, well within experimental accuracy. Burst noise is well represented by a random telegraph wave.

Burst noise may also have multiple levels as depicted in Fig. 3-1a. For a device in which two levels of burst noise are present, the power spectrum should show the presence of both levels. Figure 3-6 shows the power spectrum of device #123 which had two dominant burst levels. The spectrum is the superposition of two burst noise spectra of Fig. 3-4. Multiple level burst noise may be modeled as shown in Fig. 3-7 in which there is a burst noise generator for each burst level.

Functional Dependence of Burst Noise

Experimental measurements have been made to characterize the functional dependence of burst noise. Equivalent input burst voltage e_{BB} is found to have the functional dependence given below.

1. e_{BB} is independent of collector-base voltage when the transistor is in the forward active operating region;

2. Fig. 3-8 shows the variation of e_{BB} as a function of temperature with I_c constant. The functional dependence is found to be

$$e_{BB} = k_1 \exp(-T/T_o); \tag{3.4}$$

3. With temperature constant, equivalent burst voltage is related to collector current by

$$e_{BB} = k_2 (I_c)^n \quad , n \doteq 1/2 \tag{3.5}$$

as indicated in Fig. 3-9.

4. Fig. 3-10 demonstrates that the average burst rate is linearly dependent upon collector current when the temperature is constant.

$$ABR = k_3 I_c \tag{3.6}$$

Combining Eqns. 3.4 and 3.5, the overall functional dependence of equivalent burst voltage upon temperature, collector current, and base-emitter voltage is determined (27).

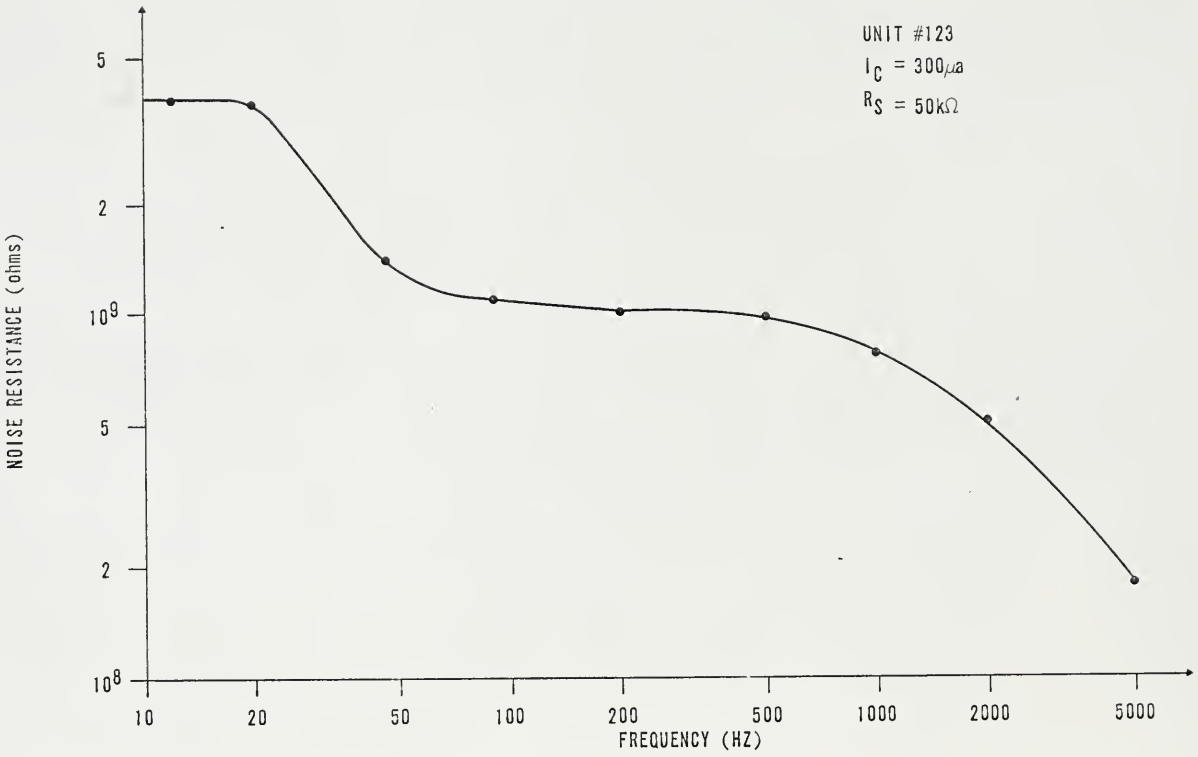


Fig. 3-6. Two level burst noise spectrum.

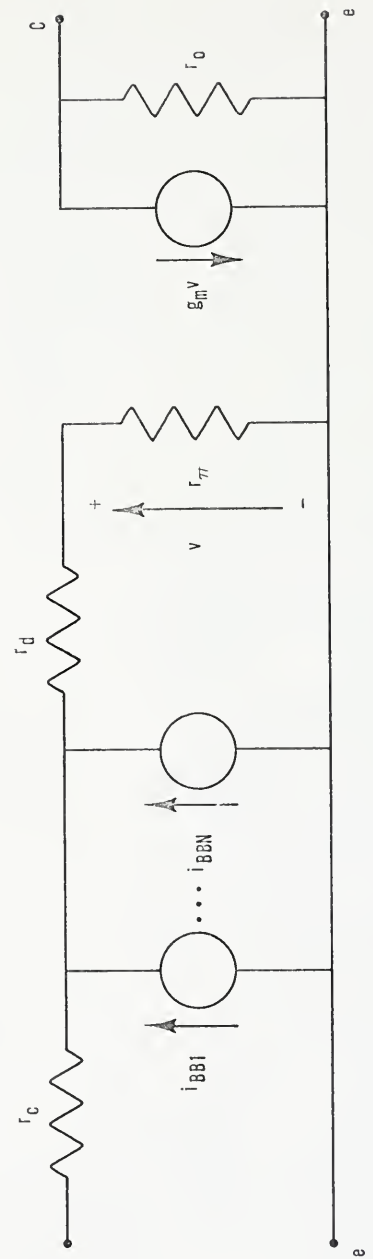


Fig. 3-7. Multi-level burst noise model.

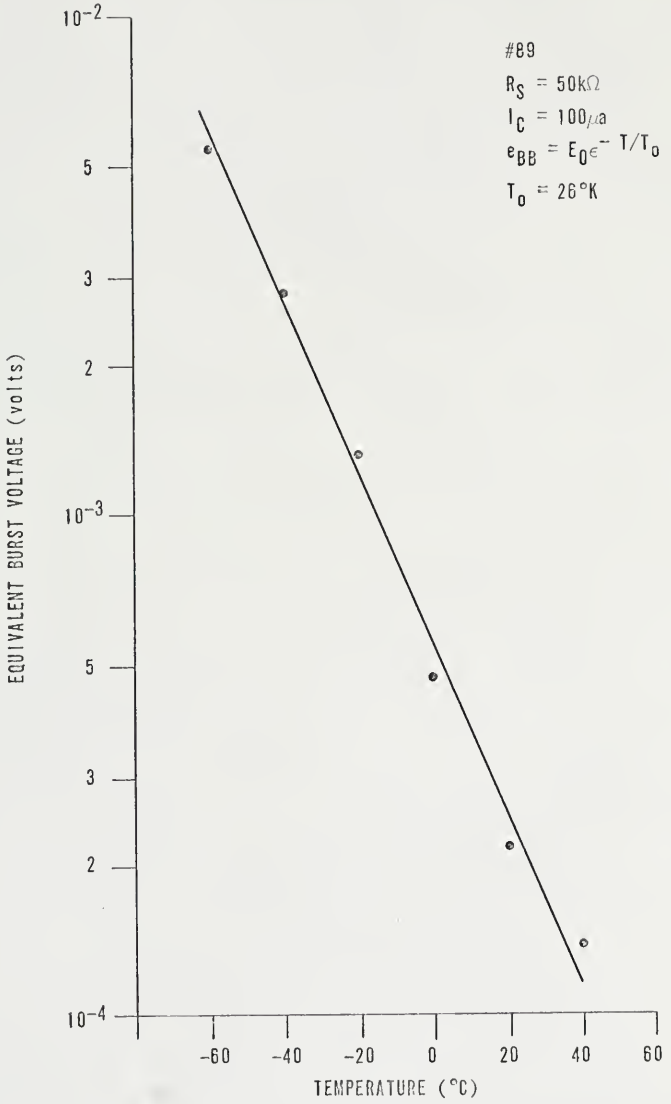


Fig. 3-8. Equivalent burst voltage versus temperature with collector current constant.

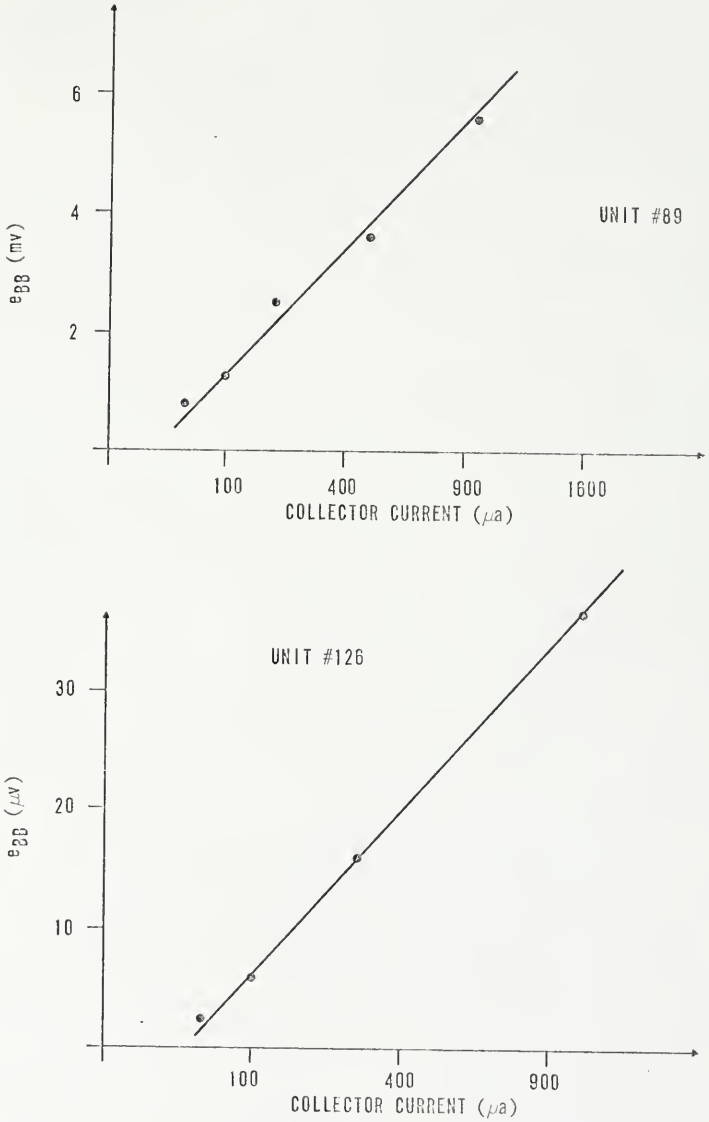


Fig. 3-9. Equivalent burst voltage versus collector current at constant temperature.

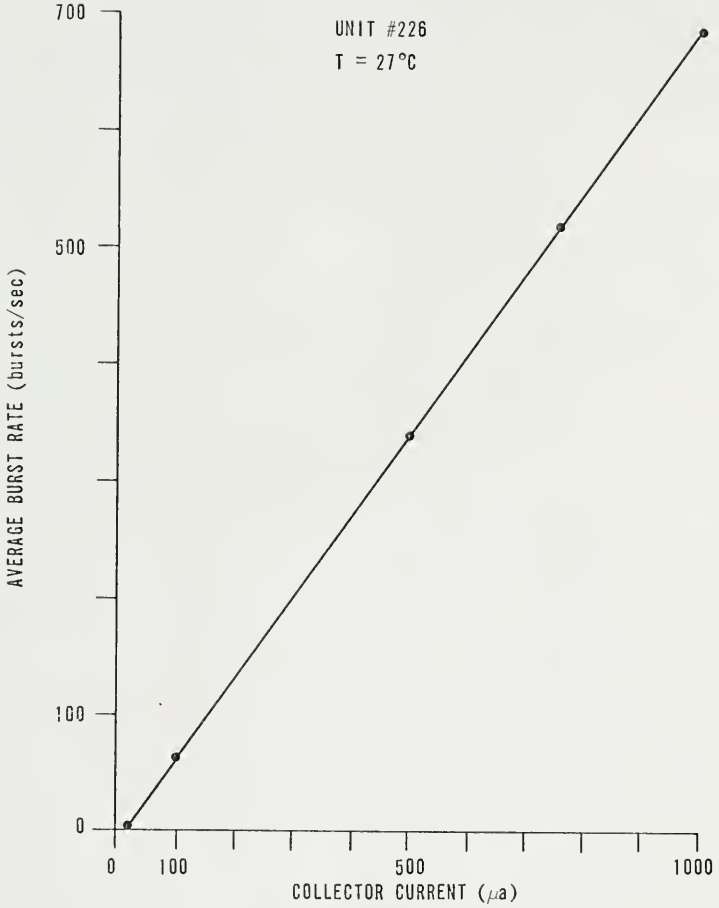


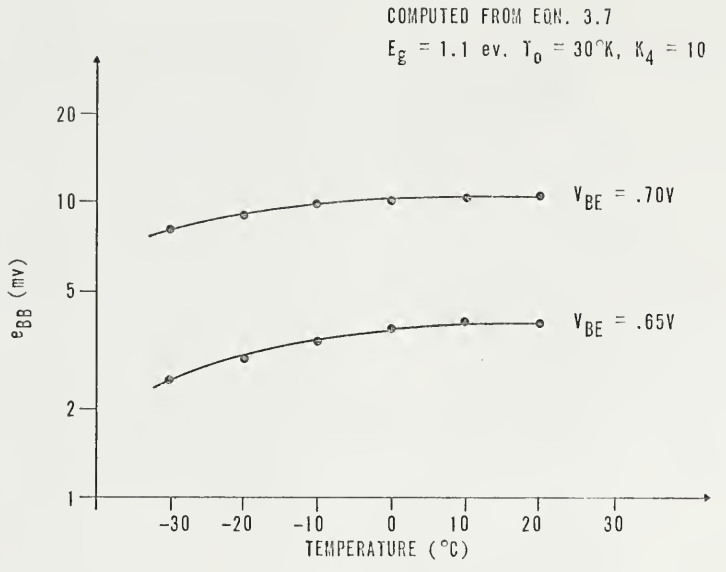
Fig. 3-10. Average burst rate versus collector current at constant temperature.

$$e_{BB} = k_4 T^{3/2} \exp(-(E_g - qV_{be})/2kT) \exp(-T/T_o) \text{ for } n = 1/2 \qquad (3.7)$$

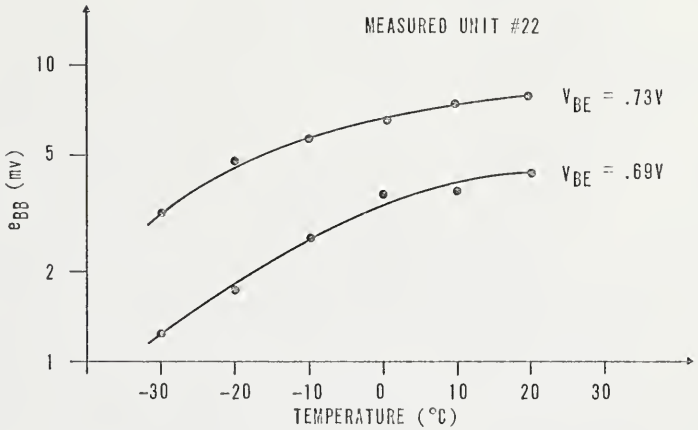
The above expression may be verified by measuring the dependence of e_{BB} upon temperature with base-emitter voltage constant. The expected variation of Eqn. 3.7 on a normalized basis is shown in Fig. 3-11a for typical values of T_o and E_g, as determined by computer analysis. Measured results are given in Fig. 3-11b showing good agreement with Eqn. 2.27.

Further study of burst noise was undertaken using the tetrode transistors discussed earlier. By varying the gate potential the carrier concentrations under the gate may be changed. As the gate potential is made more positive the base region near the surface of an npn transistor becomes more and more depleted of majority carriers. This is evidenced by a fall off in the collector current of the device (28). The units described by Fig. 3-12 had no evident burst noise until the base region of the device was sufficiently depleted. After the appearance of the burst noise, the bursts remained essentially unchanged until the surface of the base region began to invert, and then the bursts generally disappeared at this time. Burst noise appears to be intimately associated with depletion of the base region near the base-emitter junction.

Drift experiments also indicate a relationship between surface conditions and burst noise. An untreated device, unit #91, showed no bursting with the ions in the oxide drifted toward the gate. With the ions drifted to the surface, burst noise appeared. The burst noise again disappeared upon drifting the ions back to the gate.



(a)



(b)

Fig. 3-11. Equivalent burst voltage versus temperature with constant emitter-base voltage.

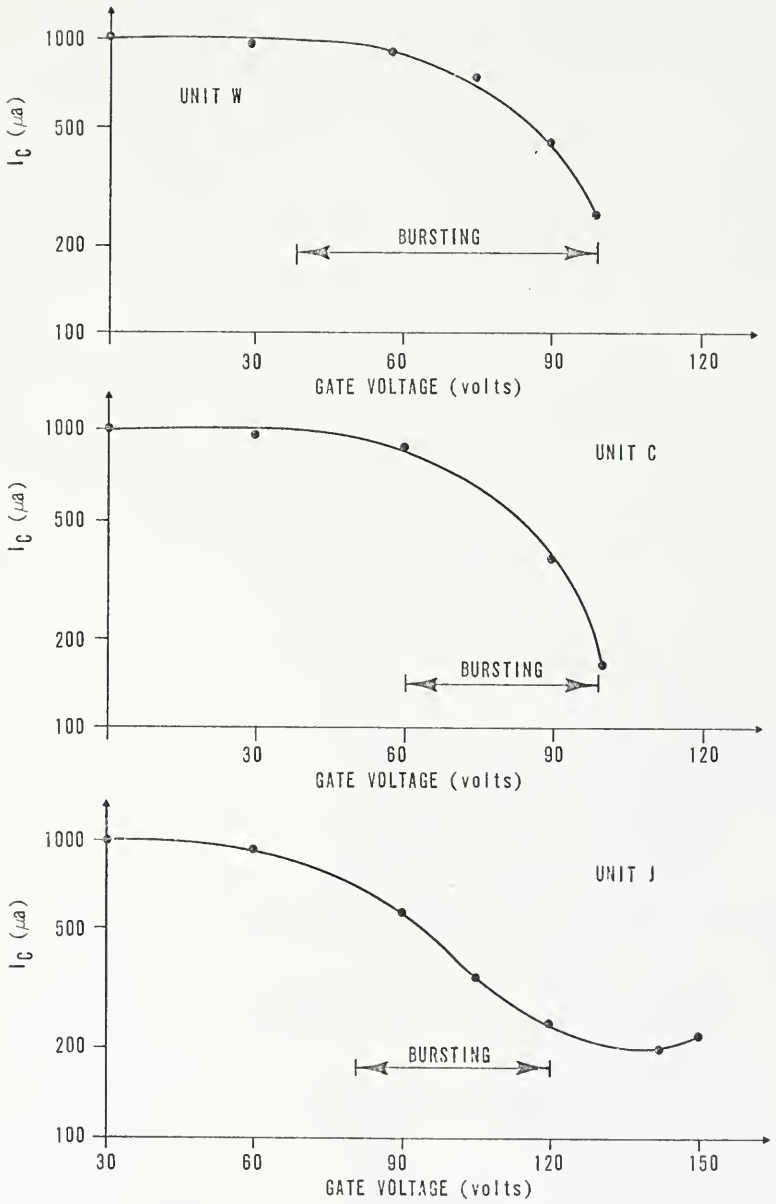


Fig. 3-12. Collector current versus gate voltage showing presence of burst noise.

Combined Spectral Effects of Burst and 1/f Noise

A model of transistor noise including a burst generator and a 1/f noise generator may be used to further explain observed noise spectra. Using the model of Fig. 3-13, the noise figure may be computed to be

$$F = 1 + k_1 f_c/f + k_2/(1 + (\pi f/2a)^2) \quad . \tag{3.8}$$

For the proper relationship between constants k_1 and k_2, the noise figure spectrum of Fig. 3-14 may be obtained. The burst and 1/f noise regions are clearly defined. The above effect is demonstrated in the spectrum presented in Fig. 3-15. The spectrum of device 2N930-54 shows first a burst noise character and then a 1/f noise character as frequency is decreased. Many transistors show the presence of significant components of both 1/f noise and burst noise, and the spectrum of Fig. 2-28 can often occur.

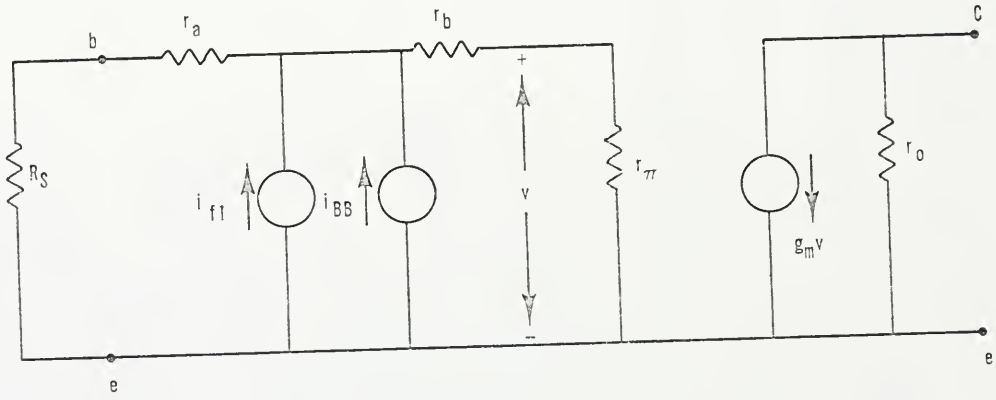


Fig. 3-13. Noise model including 1/f surface noise and burst noise generators.

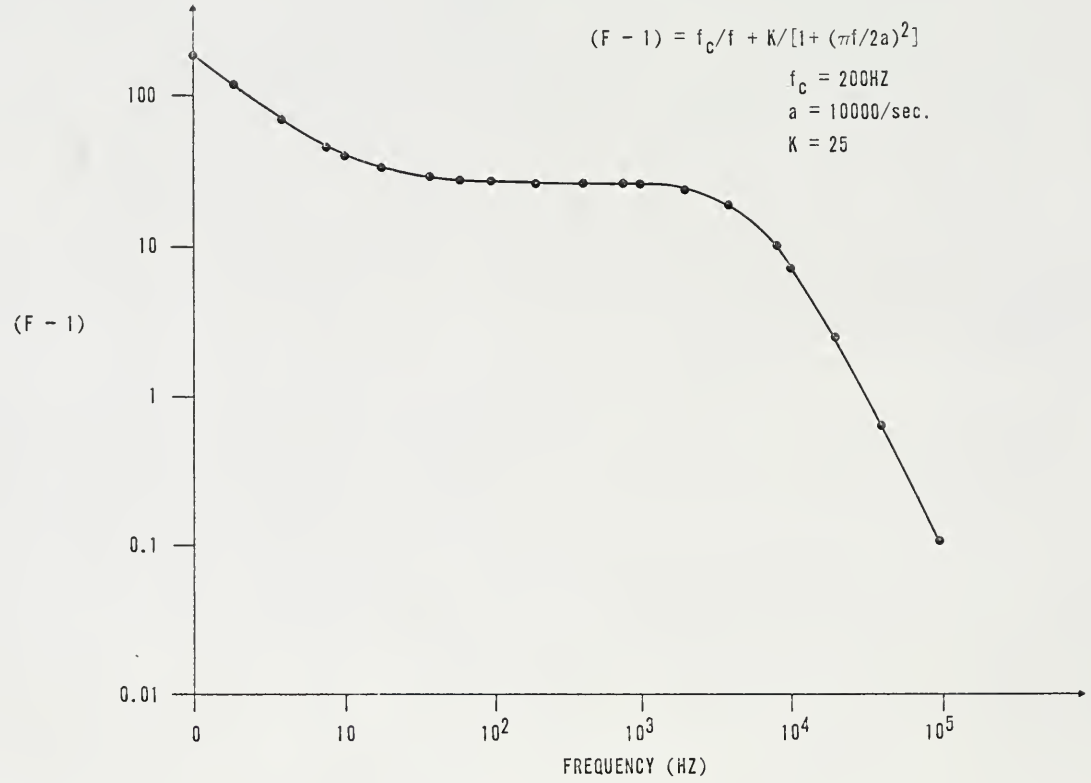


Fig. 3-14. Structured spectrum predicted by model including burst noise and 1/f noise.

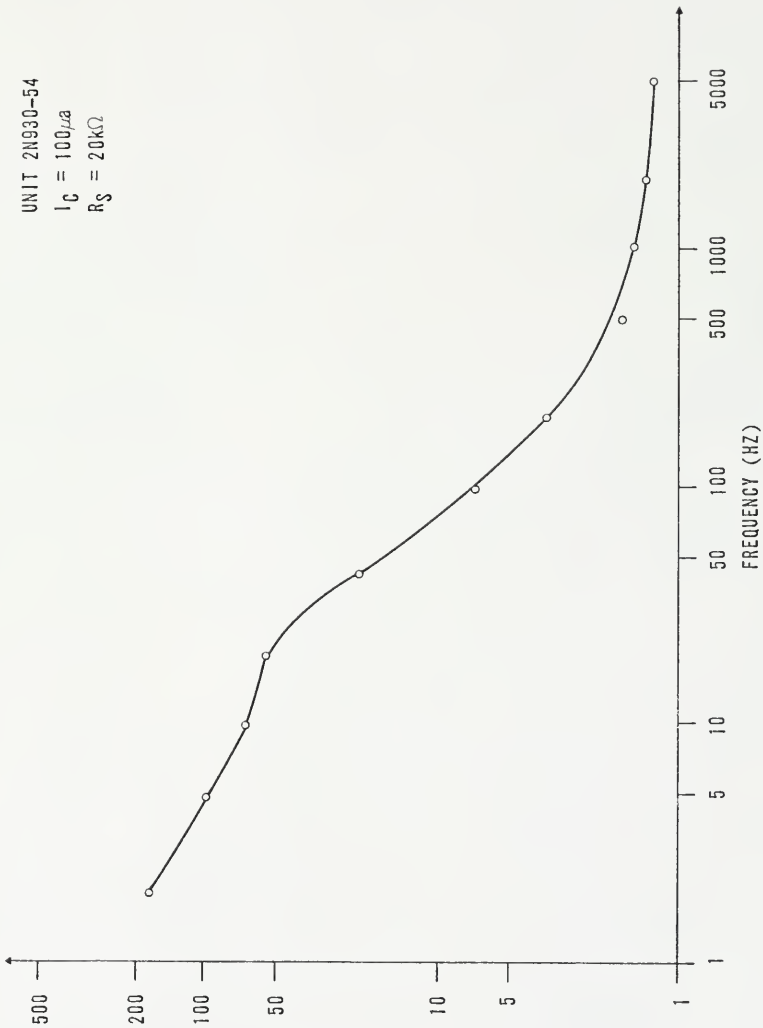


Fig. 3-15. Noise figure versus frequency showing structured spectrum.

CHAPTER FOUR

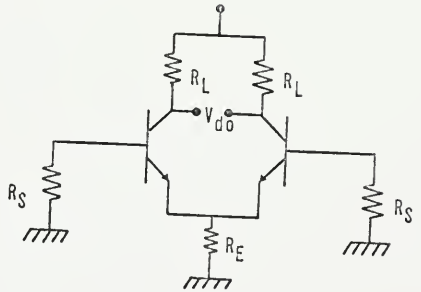
LOW NOISE AMPLIFIERS

Any noise source associated with an amplifier may reduce the sensitivity of that amplifier. At low frequencies, burst noise and 1/f noise are most significant in reducing the sensitivity of an amplifier. Methods of controlling burst and 1/f noise are discussed below, and a new low noise amplifier is proposed.

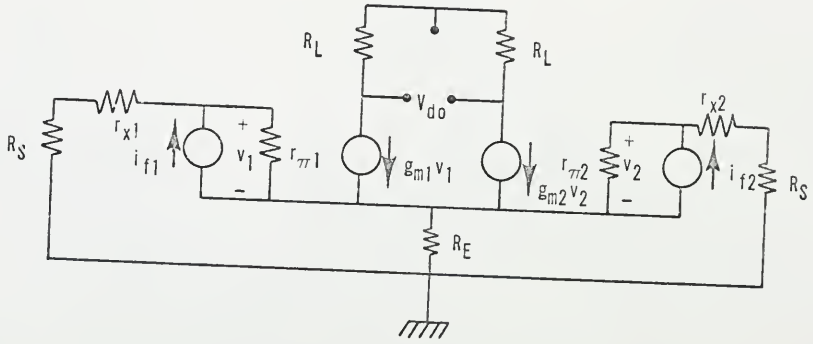
Because of the proximity of devices in integrated circuits, thermal coupling between devices has been postulated as a possible source of correlation of the 1/f noise sources in adjacent transistors in integrated circuits (29). The differential amplifier of Fig. 4-1a is ideal for studying the possible correlation of 1/f noise sources in devices. Using the small signal equivalent circuit of Fig. 4-1b, the differential output noise is found to be

$$\overline{v_{do}^2} = (\beta_o R_L R'_s/(R_s+r_\pi))^2(\overline{i_{f1}^2} + \overline{i_{f2}^2} - \overline{i_{f1}^* i_{f2}} - \overline{i_{f1} i_{f2}^*}) \quad . \tag{4.1}$$

Positive correlation could improve the noise performance of the transistor differential amplifier. If no correlation is present, other amplifier configurations must be studied in order to find a method of controlling noise.



(a)



(b)

Fig. 4-1. Transistor differential amplifier and small signal equivalent circuit.

Fig. 4-2 shows the noise spectra of two matched transistors of the transistor array CA-3018-G. The lower spectral curves are of transistors 345 and 678 of the above array operated separately in the common emitter connection. The upper spectrum is of the same transistors operated in the differential amplifier configuration. Close examination shows that the upper curve is the sum of the lower two, indicating that the noise of the two transistors in the differential amplifier adds quadratically. Thus no correlation is present in these transistors throughout the spectrum measured.

The transistor amplifier of Fig. 4-3 provides an amplifier in which 1/f, burst, and shot noise can be controlled. The small signal model of Fig. 4-4 is used to analyze the noise performance of this stage. The generators i_{n1} and i_{n2} can represent either 1/f, shot, or burst noise generators depending upon the choice of the base resistors r_a, r_b, r_c, and r_d. The components of load current caused by the noise generators i_{n1} and i_{n2} are given below.

$$i_1/i_{n1} = \frac{\beta_o(R_s+r_a+r_{\pi 2}+r_{x2}+\beta_o(R_s+r_a)-r_b-r_{\pi 1})}{R_s + r_{x1}+r_{\pi 1} +(\beta_o+1)(r_{x2}+r_{\pi 2})} \qquad (4.2)$$

$$i_1/i_{n2} = \frac{\beta_o(\ (\beta_o+1)r_c -R_s -r_{x1} +r_{\pi 2} +r_d - r_{\pi 1})}{R_s + r_{x1} + r_{\pi 1} + (\beta_o+1)(r_{x2} + r_{\pi 2})} \qquad (4.3)$$

For the proper choice of the collector current ratio

$$I_{c1}/ I_{c2} = r_{\pi 2} / r_{\pi 1} \quad \text{for } \beta_o \text{ constant} \qquad (4.4)$$

the load current component caused by i_{n1} or i_{n2} may be set to zero.

$$i_1 / i_{n1} = 0 \qquad \text{for}$$

$$I_{c2}/ I_{c1} = 1+((\beta_o+1)\ (R_s+r_a) - r_b + r_a)/r_{\pi 2} \qquad (4.5)$$

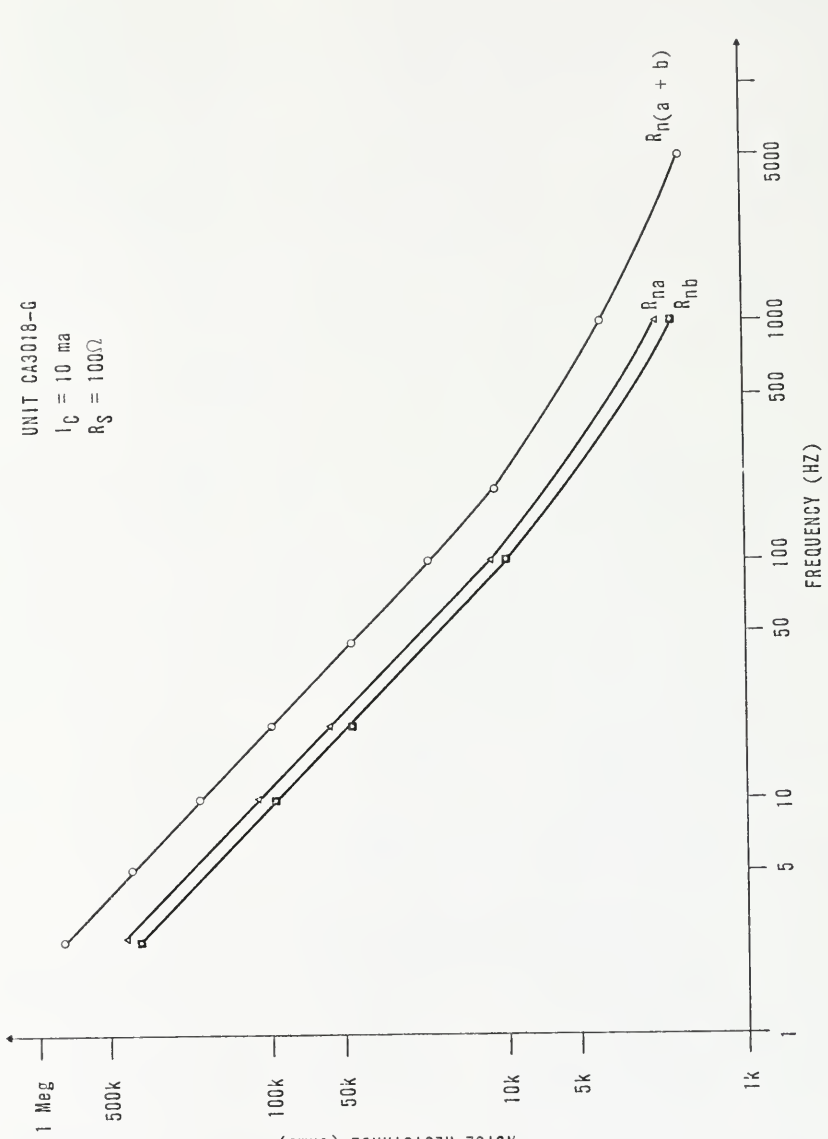


Fig. 4-2. Equivalent noise resistance versus frequency of the differential amplifier.

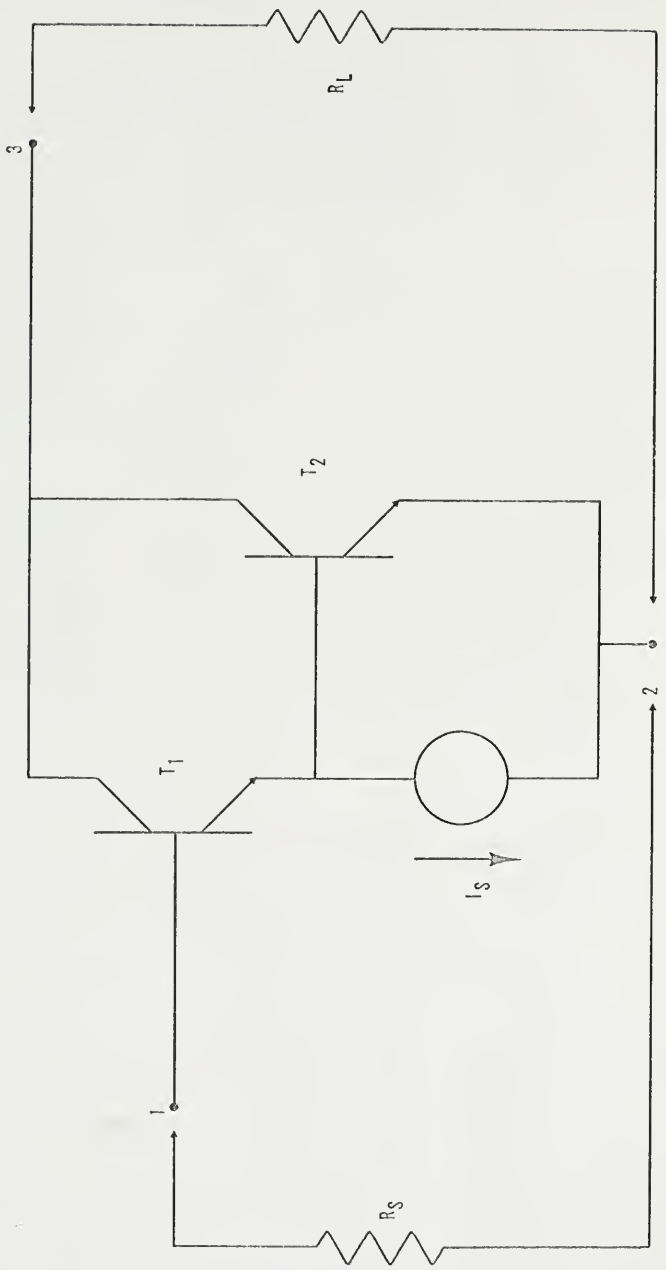


Fig. 4-3. Low noise amplifier configuration.

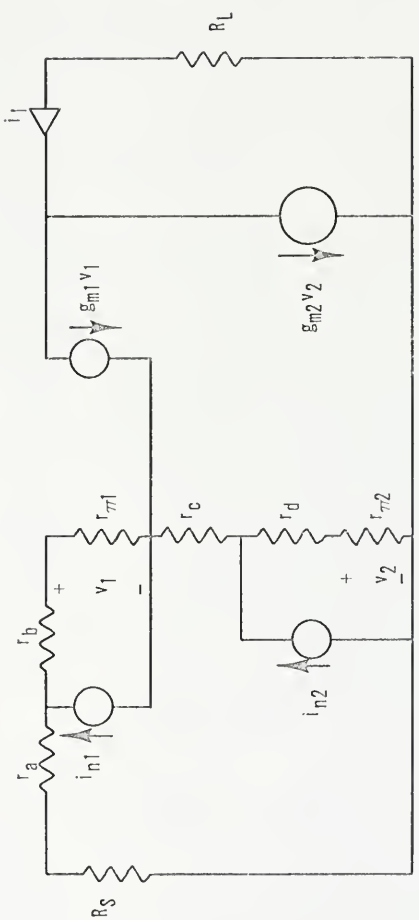


Fig. 4-4. Small signal model of the low noise amplifier.

$$i_1 / i_{n2} = 0 \qquad \text{for}$$

$$I_{c2} / I_{c1} = 1 + \beta_o r_c / r_{\pi 2} \quad -(R_s + r_{x1} - r_{x2}) / r_{\pi 2} \tag{4.6}$$

The current source of Fig. 4-3 may be adjusted for the desired collector current ratio required to remove the desired noise component from the output current of the amplifier. This technique may be used to remove burst noise, 1/f noise, and shot noise components of load current. The noise resistance of this amplifier is then basically limited by the thermal noise of the base resistances r_{x1} and r_{x2} plus the shot noise of the collector current I_{c2} since the noise of these generators cannot be affected in this configuration. The voltage gain of the configuration of Fig. 4-3 is found to be

$$A_v = \beta_o(\beta_o+2)R_1 / (R_s + r_{x1} + r_{\pi 1} + (\beta_o+1)(r_{x2}+r_{\pi 2})) \tag{4.7}$$

which is approximately equivalent to that of a common emitter amplifier stage operating with a small source resistance. Analysis of the frequency response of the amplifier of Fig. 4-3 finds that it is comparable to that of the common emitter stage also as shown in Table 4-1.

TABLE 4-1

GAIN AND BANDWIDTH OF THE LOW NOISE AMPLIFIER

	$R_s = .01$		$R_s = .1$	
	Gain	Bandwidth	Gain	Bandwidth
C-E	189	.406	161	.127
Multiple Transistor Amplifier	98	.44	98	.2

The amplifier of Fig. 4-3 can provide excellent noise performance at low frequencies in trade for a loss of gain without sacrificing bandwidth performance as compared to a common emitter stage operating under equivalent conditions.

The use of the amplifier to control burst noise is demonstrated in Fig. 4-5. The theoretical and measured curves of burst noise load current versus collector current I_{c1} are shown in this figure for the cases in which transistor T_1 is bursting and then in which T_2 is bursting. The results show that the burst noise may be eliminated by proper selection of the collector current I_{c1}.

The same amplifier configuration should provide effective control of 1/f and shot noise also. Dramatic evidence of this is presented in Fig. 4-6. The noise spectrum of the amplifier is shown for various values of collector current I_{c1}. By adjusting I_{c1} for a noise minimum, a reduction of noise figure from 1040 to 6 is obtained at a frequency of 20 Hz. The breadth of this null is shown in Fig. 4-3 indicating that adjustment of I_{c1} is not extremely critical. The results above indicate that the transistor amplifier of Fig. 4-7 may be used to produce very low noise amplifiers for low frequencies through proper amplifier adjustment and transistor matching and selection.

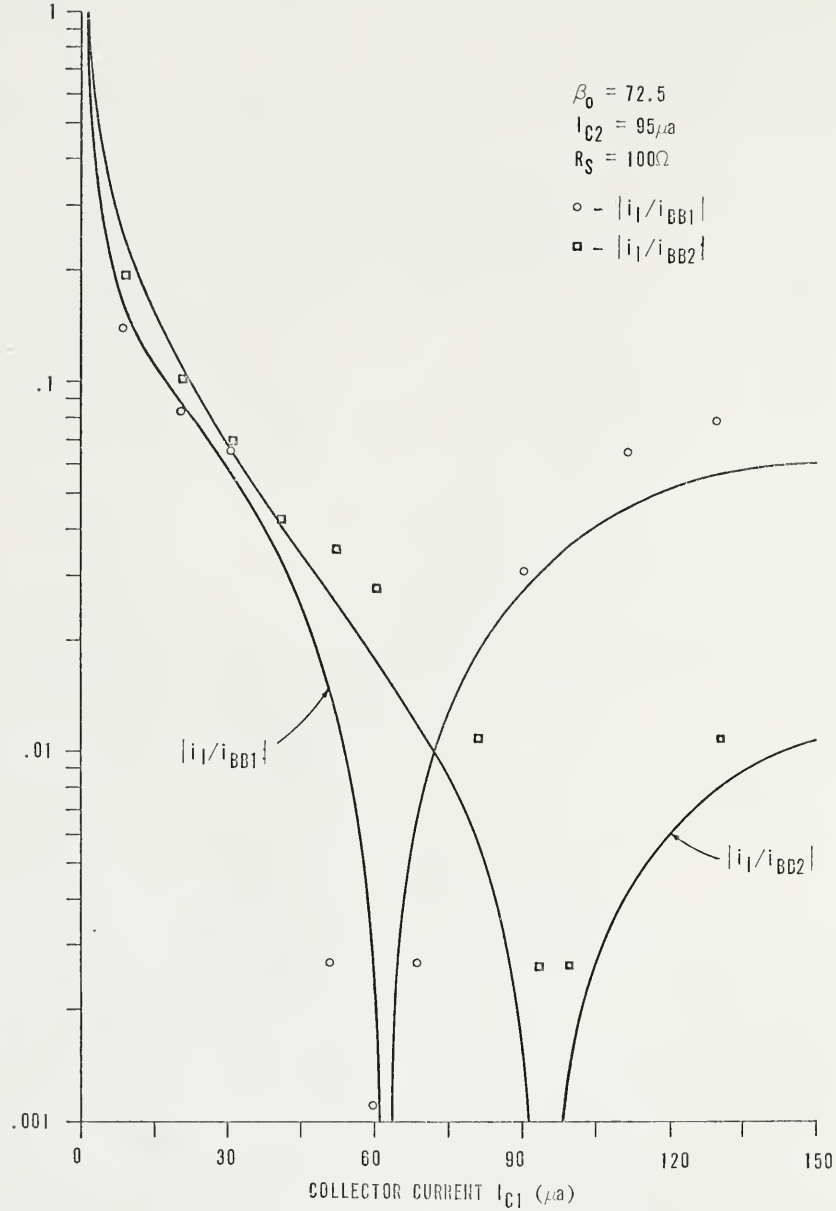


Fig. 4-5. Theoretical and experimental burst noise reduction using the low noise amplifier.

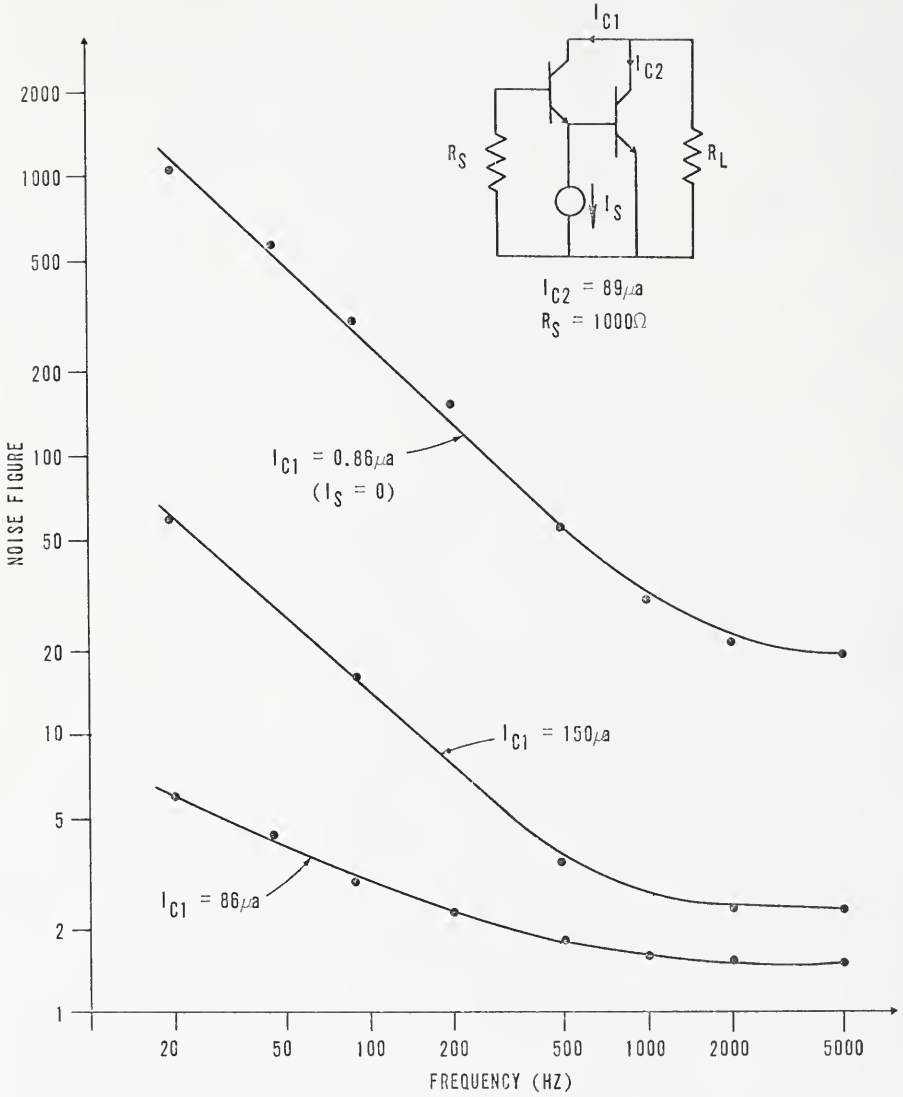


Fig. 4-6. Noise figure reduction using the low noise amplifier.

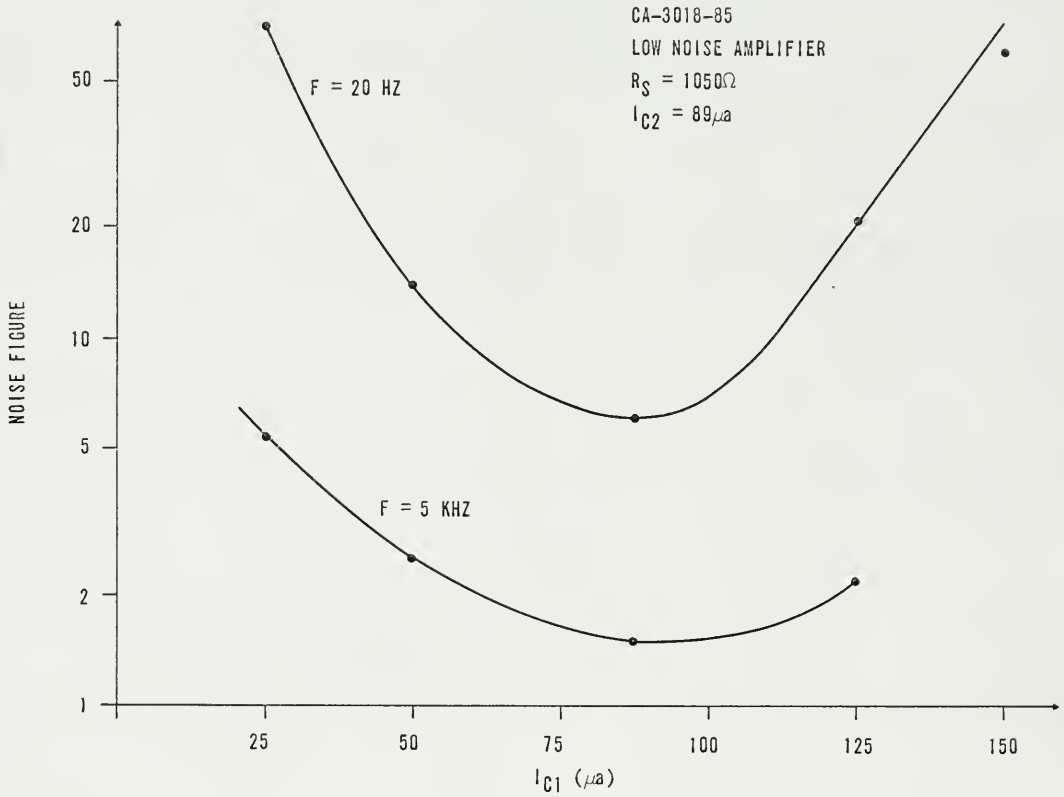


Fig. 4-7. Noise figure versus collector current for low noise amplifier.

CHAPTER FIVE

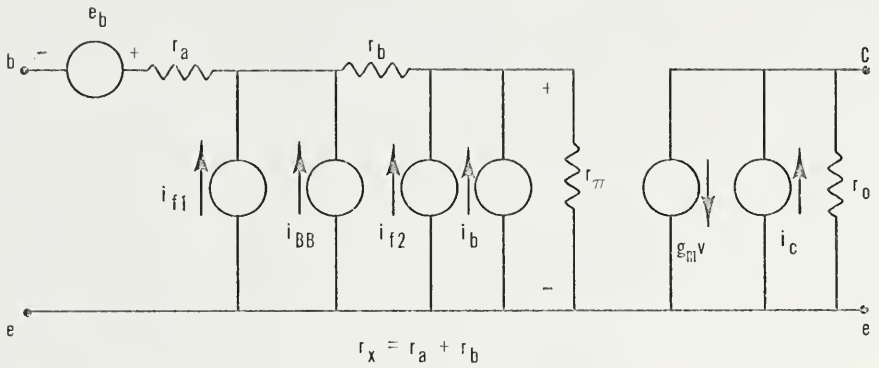
CONCLUSIONS AND RECOMMENDATIONS

The preceding work has produced several results which are discussed below.

1. Burst noise has been studied and the phenomenon characterized. Burst noise in bipolar junction transistors has been shown to be associated predominantly with the base-emitter junction and with the depletion of the surface of the base region near this junction.

2. The existence of two 1/f noise generators has been demonstrated. One noise generator has been shown to be associated with the surface noise of the emitter-base junction of the transistor. The second 1/f noise generator is associated with the active base region of the transistor. The presence of the second 1/f noise generator as speculated by Gibbons has been shown to exist.

3. An improved model of the low frequency noise of the bipolar junction transistor has been developed and is illustrated in Fig. 5-1. The model includes the shot and thermal noise generators plus two 1/f noise generators and the burst noise generator discussed above. The sum of the resistances r_a and r_b of the model of Fig. 5-1 represents the total base resistance of the transistor in question, and the resistor r_a is the resistance of the material of the inactive base region of the transistor.



$$\overline{i_c^2} = 2qI_c df \qquad \overline{i_{f1}^2} = [K_1 I_B^{\gamma_1} df]/f^{\gamma_1}$$

$$\overline{i_b^2} = 2qI_B df \qquad \overline{i_{f2}^2} = [K_2 I_B^{\gamma_2} df]/f^{\alpha_2}$$

$$\overline{e_b^2} = 4kTr_x df$$

$$\overline{i_{BB}^2} = K_3\, df/[1 + (\pi f/2a)^2]$$

Fig. 5-1. Improved low frequency noise model including two 1/f noise generators and the burst noise generator.

4. A low frequency low noise amplifier configuration has been demonstrated. Effective control of burst noise is possible through the use of the amplifier of Fig. 5-2. The same amplifier configuration can be used to realize amplifiers having very low equivalent noise resistances at low frequencies. The noise resistance of the above amplifier is basically limited by only the base resistances of the transistors used to build the amplifier and by the shot noise of the collector current of the transistor T_2 of Fig. 5-2.

5. The improved noise model has been used to predict and explain the existence of structuring of noise spectra which have been observed but have remained unexplained until this time.

Several areas which deserve further study have originated as a result of this research and are discussed below.

1. The preceding work has demonstrated the existence of a 1/f noise source associated with the active base region of bipolar junction transistors. The origin of this 1/f noise source needs to be determined.

2. Further study of burst noise is indicated. The physical cause of burst noise deserves investigation with the hope that this will lead to methods of process oriented control of the burst noise phenomenon.

3. The low noise amplifier developed in Chapter Four deserves further study. The possibility of realizing a very low noise amplifier at low frequencies is most stimulating. The configuration appears to be amenable to integration, and in fact much of its performance is due to the matching which can be obtained between devices in integrated

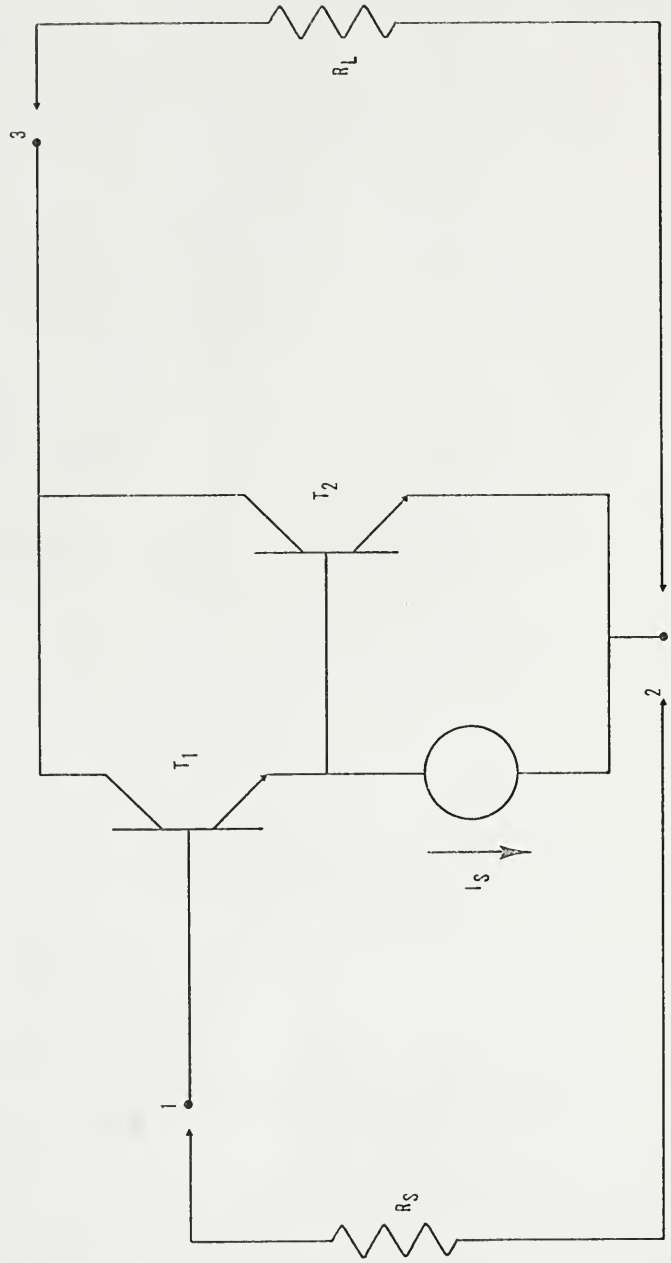


Fig. 5-2. Low noise amplifier configuration.

circuits. It is recommended that this amplifier configuration be exhaustively studied.

APPENDIX

MEASUREMENT SYSTEMS AND METHODS

The results of Chapters Two, Three, and Four were obtained using the systems described in this Appendix. Two major systems are described which can be used to determine noise resistance, noise figure, and equivalent burst noise voltage. Other minor systems are described, and methods of measuring transistor parameters developed. The system used to measure noise resistance was described in Chapter Two. The block diagram of this system is shown in Fig. A-1.

The actual measurement system is shown in Fig. A-2. A Hewlett-Packard HP-141 oscilloscope is used as the system's variable gain amplifier and to monitor the noise output of the device under test. Following this amplifier is a monitor oscilloscope which is used to insure that no clipping of the noise occurs in the main amplifier. The filter and quadratic detector are contained in a Quan-Tech wave analyzer. This wave analyzer tunes from 1 Hz to 5 kHz with bandwidths of 1 Hz, 10 Hz, and 100 Hz with a full scale sensitivity of 30 V to 100 volts rms. The wave analyzer permits the selection of four meter time constants of 0.1, 1, 10, and 100 seconds, providing excellent averaging capability. A dc analog recorder output drives a chart recorder which is used to provide accurate determination of a given meter level. The calibration signal is derived from the BFO output of the wave analyzer

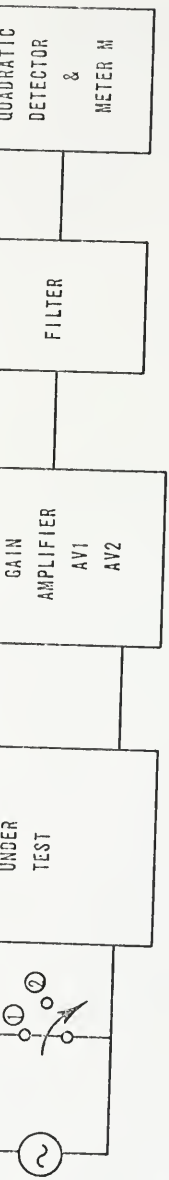


Fig. A-1. Basic noise measurement system.

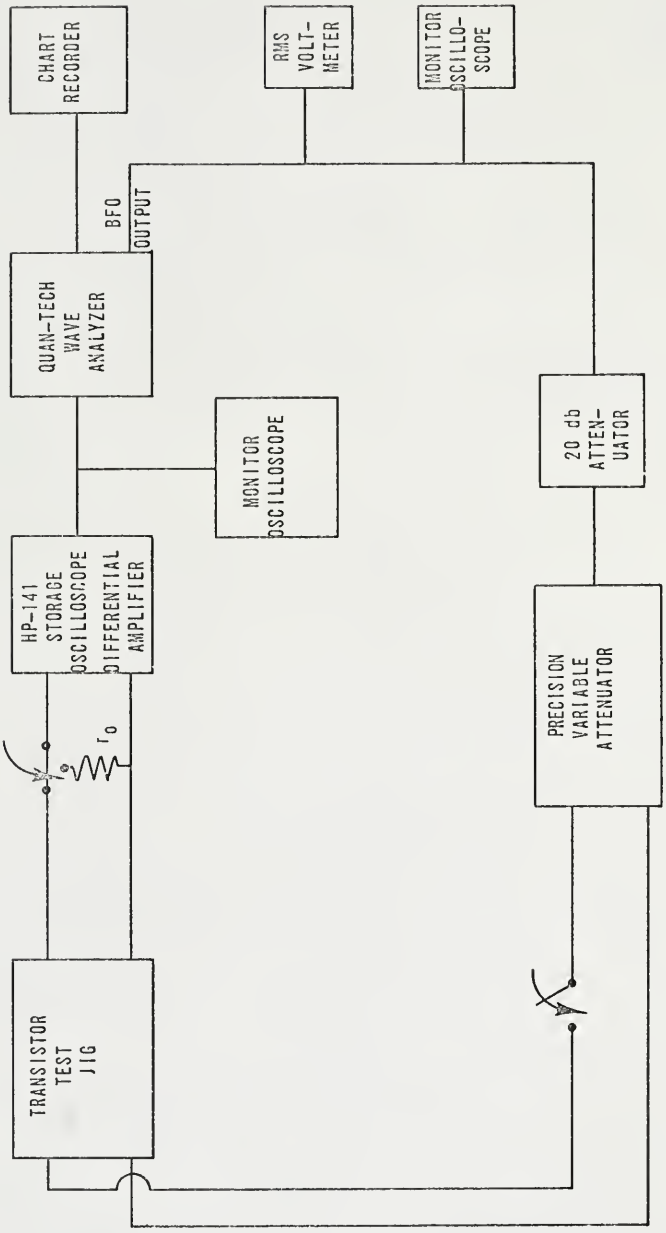


Fig. A-2. Actual noise measurement system.

and is set to one volt rms. This signal is monitored on a voltmeter and oscilloscope, and it is followed by variable attenuation to provide an adjustable calibrating signal.

Use of the system is as follows. With the calibrating switch open, the noise in a particular frequency range is measured with a given amplifier gain setting, and the detector reading is recorded. The main amplifier gain is then reduced by an arbitrary factor (100 times for example). The calibrating signal is introduced by closing the calibrating switch, and the attenuator is adjusted until the original detector level is attained as monitored on the recorder. The equivalent noise resistance is then given by:

$$R_n = 1/[(1-(AV2/AV1)^2)(4kTdf)\ (\text{antilog}(\text{total system attenuation in db}/10))] \quad . \qquad (A.1)$$

In the above expression, AV1/AV2 is the ratio of the main amplifier gain settings, and the total system attenuation also incorporates this figure. An accurate knowledge of the effective noise bandwidth df is necessary to provide accurate measurement of noise resistance using the above system. The filter characteristics of the wave analyzer were experimentally measured, and the effective noise bandwidth was determined by numerical integration. The results of this process yielded effective noise bandwidths of 1.23 Hz, 12.5 Hz, and 125 Hz, for the 1 Hz, 10 Hz, and 100 Hz bandwidth settings of the wave analyzer respectively. Also affecting the accuracy of the system is the background noise of the main amplifier and wave analyzer. Therefore, continual checks must be made in order to insure that the background noise of the system is negligible with respect to the output noise of the device under test.

This is accomplished by connecting a resistor, equivalent to the output resistance of the transistor under test, across the input of the main amplifier. As long as the rms value of the noise voltage measured under these test conditions is less than one-tenth of that during the measurement of the transistor under test, then the error in measurement of the equivalent noise resistance R_n, introduced by system noise, will be less than one percent.

The transistor under test is mounted in the test jig of Fig. A-3. The circuit consists of a fixed attenuator and transistor biasing circuitry. The source resistance of the transistor is easily controlled in this circuit, and the attenuator circuit provides both attenuation and matching for the variable attenuator. Also the value of the biasing resistor R_B may be varied between wide limits without affecting either the value of source resistance R_s as seen by the transistor or the precision of the fixed attenuator.

The second measurement system is the system of Fig. A-4 which is used to measure equivalent burst voltage e_{BB}. The system consists of the transistor under test, the HP-141 oscilloscope and a calibrating signal. The oscilloscope is again used as a variable gain amplifier, and the storage capability is used to measure burst amplitude. The calibrating signal consists of a signal source adjusted to yield a one volt peak-to-peak amplitude followed by a variable attenuator. The test jig is the same as that of Fig. A-3 which provides attenuation, matching for the variable attenuator and biasing.

With the calibrating signal off, the burst amplitude at the output of the transistor under test is stored and its amplitude determined. The

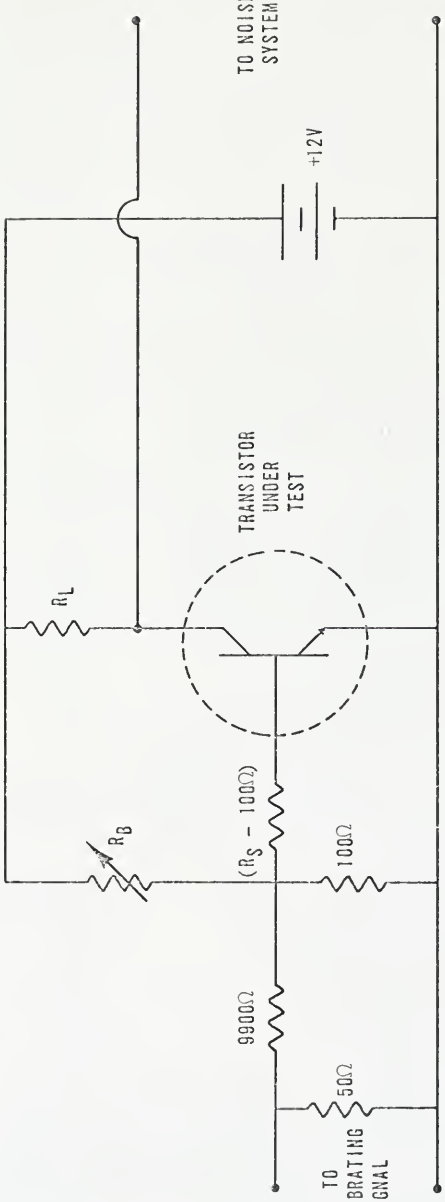


Fig. A-3. Transistor test jig.

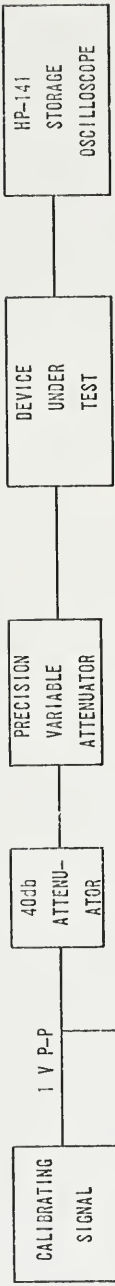


Fig. A-4. Burst noise measurement system.

system gain is then reduced by a convenient factor (100 for example), and the calibrating signal is adjusted to provide a signal of the same amplitude at the output of the transistor under test. The equivalent input burst voltage e_{BB} is given by:

$$e_{BB} = 1/[\text{antilog}(\text{total system attenuation in db}/20)] \quad . \tag{A.2}$$

Again the total system attenuation includes the ratio of the amplifier gains.

The above two systems may be used to provide measurements of equivalent noise resistance versus source resistance and frequency, and measurements of equivalent burst voltage as a function of source resistance, temperature, and operating point.

Measurement of the average burst rate utilizes the system of Fig. A-5. The burst output of the transistor under test is amplified and passed through the infinite limiter which removes the background noise from the bursts. The clean bursts are then counted by the counter, and the average burst rate determined. The infinite limiter is realized using an analog computer and the circuit of Fig. A-6.

Measurement of β_o is accomplished using the circuit of Fig. A-7. With a small signal applied from the source, the adjustable resistance R is varied to yield a null on the detector. When the null is reached, β_o is given by

$$\beta_o = (R_1 - h_{ie})/R \quad . \tag{A.3}$$

Precision potentiometers are used to provide accurate measurement of β_o, and a wave analyzer is used to provide a signal source and detection.

In order to help characterize the small signal models developed in Chapter Two, the low frequency short circuit input impedance

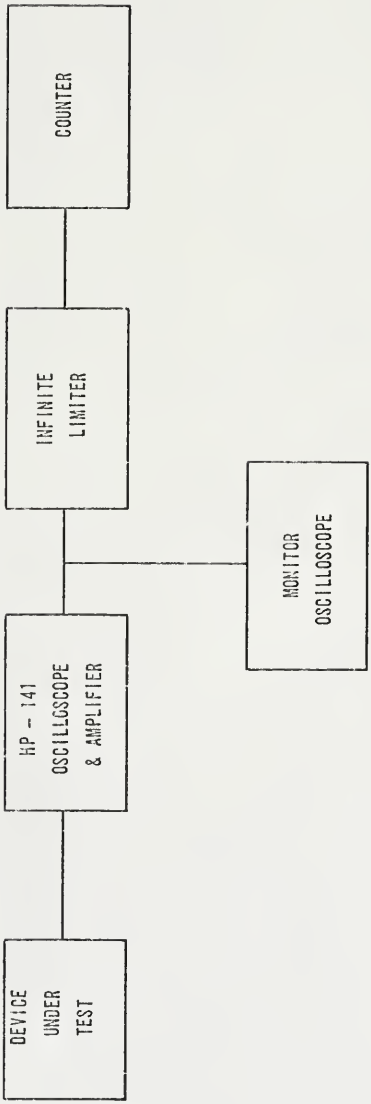


Fig. A-5. Burst rate measurement system.

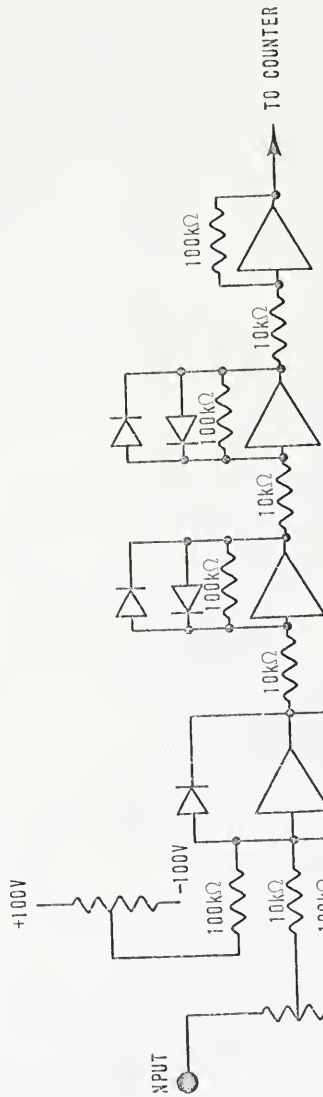


Fig. A-6. The infinite limiter.

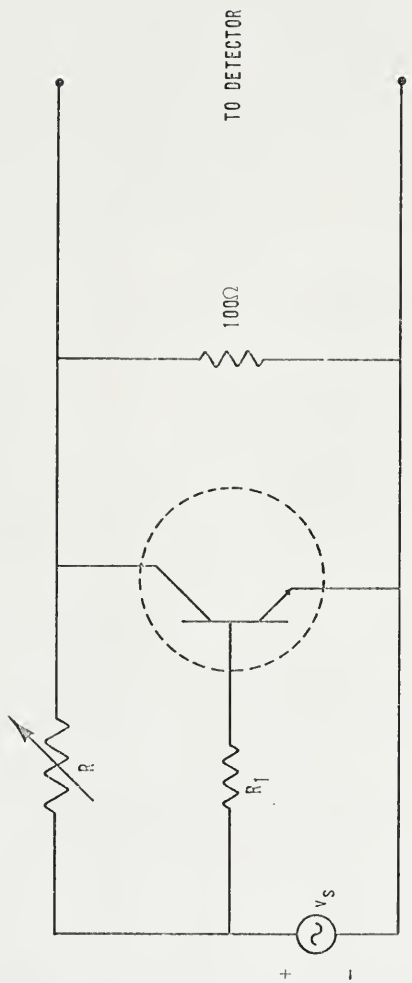


Fig. A-7. Method of beta measurement.

$$h_{ie} = r_x + r_\pi \qquad (A.4)$$

must be determined. The impedance h_{ie} is measured using a Wayne-Kerr B-601 bridge utilizing the test jig of Fig. A-8. The low frequency short circuit current gain β_o of the transistor and the transistor base resistance r_x may then be determined using this value.

The standard emitter coupled pair connection of transistors is used to measure the noise of the differential amplifier. The noise measurement system of Fig. A-1 is used except that the scope amplifier is now used in its differential input mode. The equivalent noise resistance of the emitter coupled pair is then referred to the input of one of the transistors of the pair as shown in Fig. A-9. The noise of each transistor is measured separately in the common emitter connection using the measurement system of Fig. A-1 and the test jig of Fig. A-3.

The burst noise and noise resistance of the compound Darlington connection of transistors are measured using the circuitry of Fig. A-10. The collector current ratio is varied by varying the current source current control resistor R. The variation of burst noise output current and amplifier noise resistance as a function of current are determined using the two major systems described earlier.

The measurement systems of this chapter provide the instrumentation necessary to verify the theory presented in Chapters Two, Three, and Four.

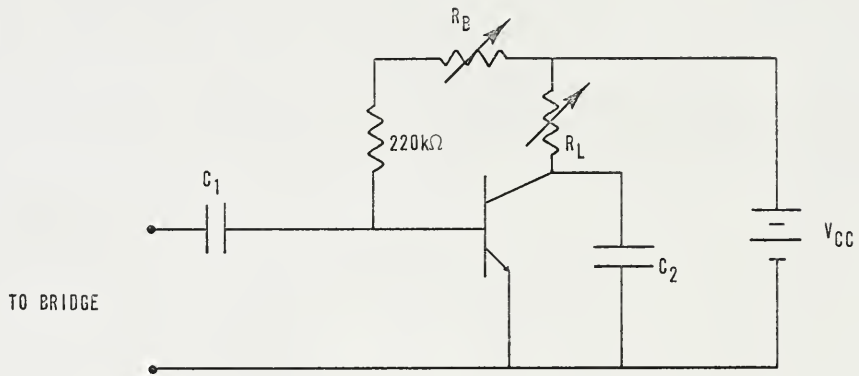


Fig. A-8. Test jig for h_{ie} measurement.

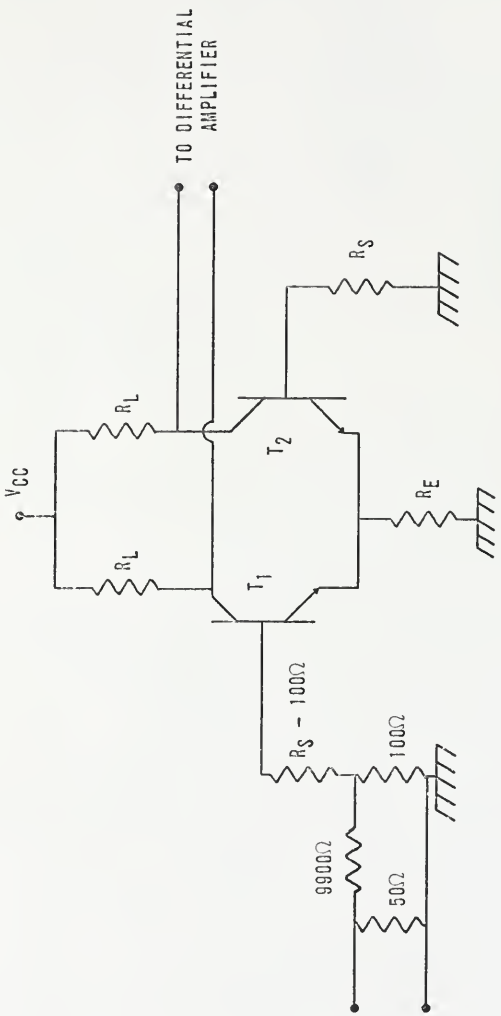


Fig. A-9. Differential amplifier test jig.

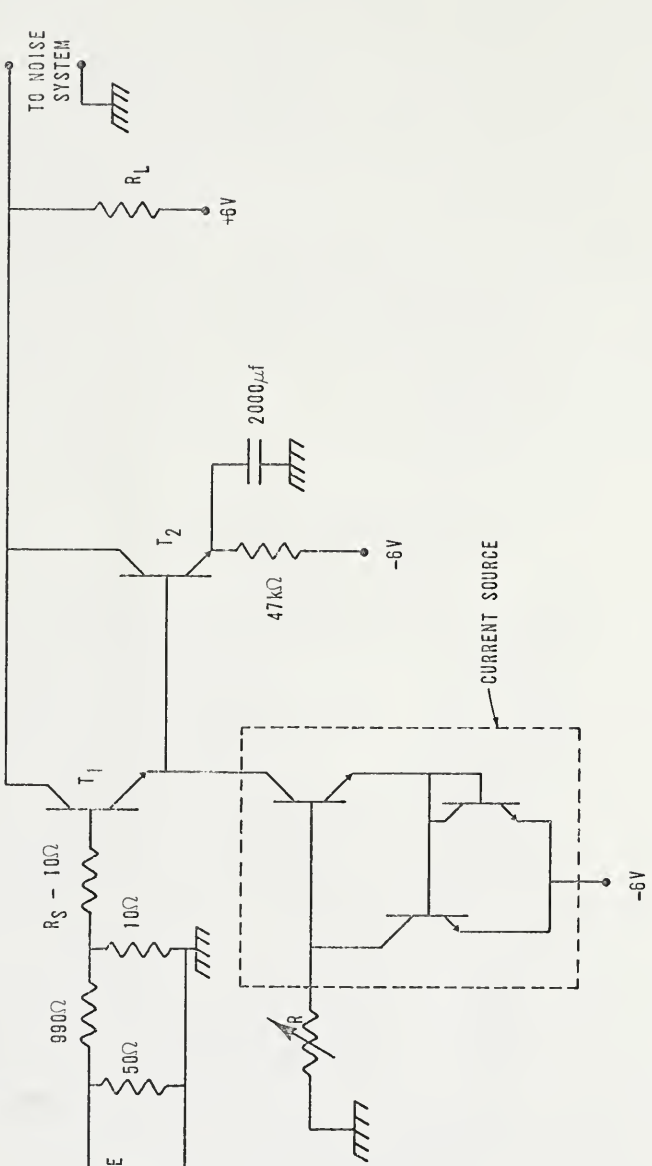


Fig. A-10. Low noise amplifier.

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BIOGRAPHICAL SKETCH

Richard Charles Jaeger was born on September 2, 1944, in New York, New York. He completed his secondary education in Fort Lauderdale, Florida, in June, 1962, and entered the University of Florida in September, 1962. He received the degree of Bachelor of Electrical Engineering with High Honors in April, 1966. Upon receiving an NDEA Title IV graduate fellowship, he entered the Graduate School of the University of Florida and was awarded the degree of Master of Engineering in December, 1966. Since that time he has pursued studies leading to the degree of Doctor of Philosophy.

Richard Charles Jaeger is married to the former Joan Carol Hill, and they have a son, Peter Charles Jaeger. He is a member of Phi Kappi Phi, Tau Beta Pi, Eta Kappa Nu, Sigma Tau, the Institute of Electrical and Electronics Engineers, and Kappa Sigma social fraternity.

This dissertation was prepared under the direction of the chairman of the candidate's supervisory committee and has been approved by all members of that committee. It was submitted to the Dean of the College of Engineering and to the Graduate Council, and was approved as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

June 1969

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